Next-generation Channel Coding towards Terabit/s Wireless Communications

André Bourdoux, IMEC

on behalf of the EPIC partners

THz Workshop - 7 March 2018, Brussels

The EPIC project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 760150.

Future Beyond 5G use cases call for 0.1- 1Terabit/s

	BER	Flexibility	Latency	Throughput [Gbps]
Virtual reality	10^-6	high	0.5ms	500,00
Data kiosk	10^-12	low	0.5ms	1000,00
Backhaul	10^-8	medium	100ns	250,00
Intra-device com.	10^-12	low	100ns	500,00
Fronthaul	10^-12	medium	25ns	1000,00
Data center	10^-12 ~ 10^-15	medium	100ns	1000,00
Hybrid wireless fiber	10^-12	medium	200ns	1000,00
High speed satellite	10^-10	medium	max ~10ms	100-1000

FEC implementation is challenging at rates 0.1-1Tb/s

FEC KPI bounds	
Area limit	10 mm²
Area efficiency limit	100 Gb/s/ mm²
Energy efficiency limit	~1 pJ/bit
Power density limit	0.1 W/mm²

High performance coding schemes in recent/emerging wireless standards

- Turbo-codes
- LDPC
- Polar codes

- Efficient implementations exist
- Perform close to Shannon limit

In depth state-of-the-art study → Gap analysis

example

	Use Case	SoA Polar Decoder Candidates					
	Fronthaul	[96]	[96]	[97]	[98]	[99]	[100]
	-	SC-U	SC-M	SC-C	SCL-U	SCL-M	BP-D
Num. of Decoders		2	21	104	48	232	65
Throughput (Gb/s)	1000	1024	1029.1	1007.4	1025.6	116.3	1013.1
Area (mm^2)	10	10	10	10	10	10	10
Power (W)	0.6	1.7	4.8	11.7	2.2	44.8	11.1
Area Eff. ($Gb/s/mm^2$)	100	102.4	102.9	100.7	102.6	11.6	101.3
Pow. Den. (W/mm^2)	0.06	0.17	0.48	1.17	0.22	4.48	1.11
Energy Eff. (pJ/bit)	0.6	1.6	4.7	11.6	2.2	385.7	11
Latency (µs)	0.025	0.4	0.5	0.1	0.3	1	0.1
Freq. (MHz)	1000	1000	1000	18.9	1000	1000	1000

example

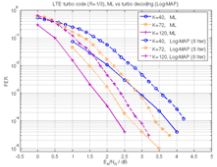
	Use case	SoA LDPC Decoder					
	Fronthaul	[78]	[80]	[82]	[83]	[89]	[90]
		LDPC-BC	LDPC-BC	LDPC-BC	LDPC-BC	LDPC-CC	LDPC-CC
		partially	fully	unrolled	unrolled	pip. WD	pip. WD
Num. of Decoders	-	48	33	3	2	84	42
Throughput (Tb/s)	1000	1005.0	1008.7	1170.0	1148.5	1005.5	1007.0
Area (mm2)	10	1.1	3.3	0.6	4.3	3.1	1.2
Power (W)	0.6	1.2	6.3	0.6	4.1	2.0	1.3
Area Eff. (Tb/s/mm2)	100	41977.2	9973.9	5641.1	531.7	27297.0	34460.0
Pow. Den. (W/mm2)	0.06	1.0	1.9	1.0	1.0	0.6	1.1
Energy Eff. (pJ/bit)	0.6	1.2	6.2	0.5	3.6	2.0	1.3
Latency (µs)	0.025	0.03	0.06	0.03	0.10	0.34	NA
Freq. (MHz)	1000	1000.0	1000.0	714.0	1000.0	1000.0	1000.0

- These are two examples. Analysis done for the seven uses cases and the three code families
- All best references where “scaled” from their original CMOS node to 7nm
- Main conclusion:
  - Throughput of 1 Tb/s is hard but not beyond reach at 7nm (parallelism is key)
  - Power, power, power! (reflected in total power, power density and energy efficiency)
  - Flexibility (in code rate and/or block length) is often difficult to combine with very high speed
  - For some use cases: latency is challenging

EPIC challenges!

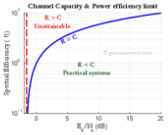
EPIC Design Framework

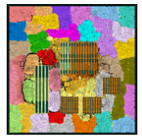
- Holistic approach
- Information theory, algorithm/architecture co-design and implementation optimization at front-end and back-end level



Codes
- Turbo
- LDPC
- Polar
- Variants….

Channel Capacity





Decoding algorithms
- ML
- Log-MAP
- Min-Sum
- Successive Cancelation
- ……

bit/frame error rates

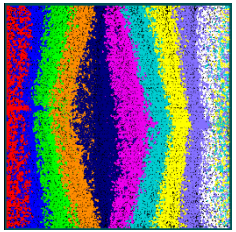
Implementation
- Semiconductor technology
- Parallel Architectures
- Error resilience
- …….

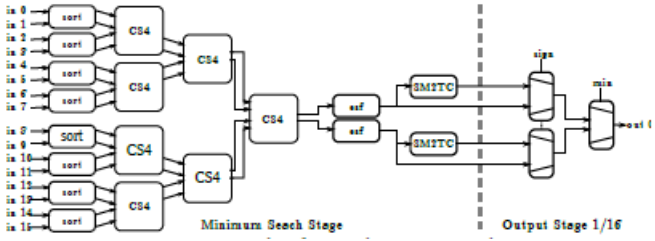
bits/s, W/mm², J/bit, bits/s/mm²

Information Theory/Implementation Gap

Energy efficient high throughput architectures require

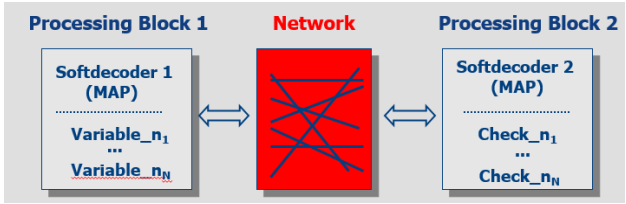
- Large parallelism
- Large regularity
- Large locality





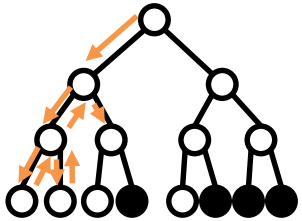
Coding theory requires randomness and no-locality

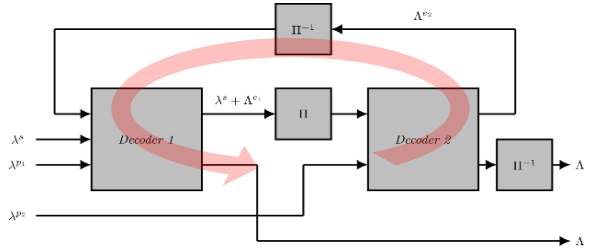
- LDPC: Tanner Graph
- Turbo Code: Interleaver



Some decoding algorithms are inherently serial

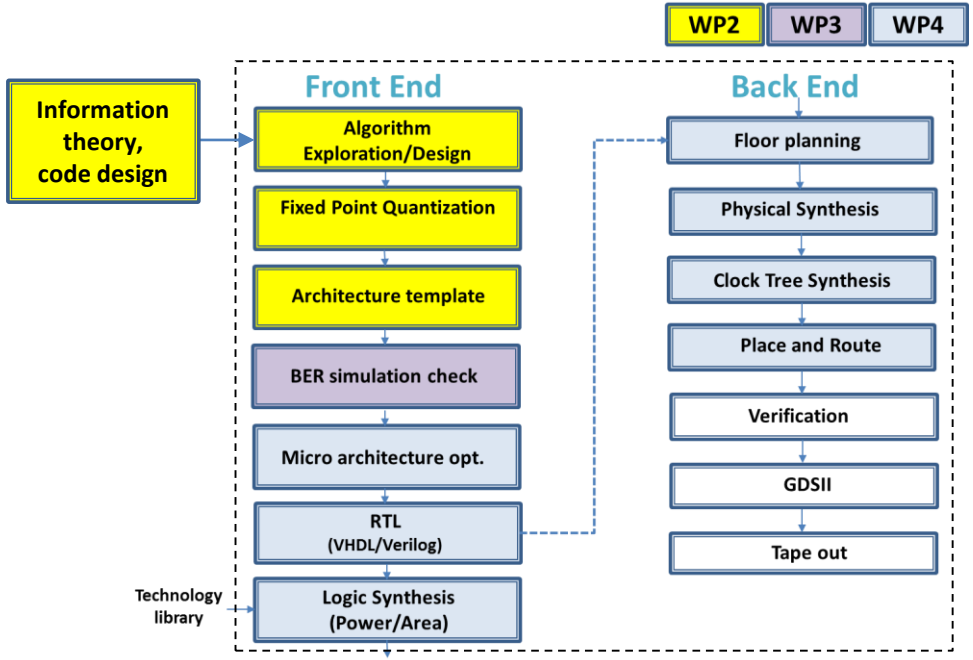
- Turbo-Code decoding
- Polar Code successive cancelation





Strong link with Silicon technology

- Information theory, algorithms, architecture and implementation in Silicon are mapped on the technical workpackages
- Selected designs will go all the way through the ASIC implementation (front-end and back-end) in deeply-scaled CMOS
- Target technology node: bulk 7nm CMOS
  - Higher clock frequency, better area efficiency, better energy efficiency



Project Goals

- The EPIC consortium is dedicated to successfully reach the following objectives
  - Design and implementation of **next generation Forward-Error-Correction** for wireless Tb/s technology and **Beyond-5G systems**
  - Advancement of **state-of-the-art channel codes** and **channel coding technology** for wireless Tb/s technology
  - **Holistic design approach** that considers code design, decoding algorithms and efficient implementation on advanced silicon technologies in a cross-layer approach
  - Validation and demonstration of new FEC technology and corresponding implementations as **virtual silicon tape-out** using realistic use cases
  - Provide **scientific excellence and contributions** to wireless industry in the domain of B5G standardization and technology development

General Project Information

- Project reference: **760150**
- Project start: **1st September 2017**
- Duration: **3 years**
- Total costs/EC contribution: **EUR 2.966.268,75**
- **Eight partners** from **seven** different **European countries:**
  - Creonic Gmbh , Ericsson AB, IMEC, Institut Mines-Telecom, InterDigital Europe, Polaran , Technikon, Technische Universitaet Kaiserslautern
- **Mission:** EPIC aims to develop a new generation of Forward-Error-Correction (FEC) codes in a manner that will serve as a fundamental enabler of practicable beyond 5G wireless Tb/s solutions and also to develop and utilize a disruptive FEC design framework allowing to advance state-of-the-art FEC schemes.
- Website: www.epic-h2020.eu

EPIC Grant Agreement No. 760150

“The EPIC project has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreement No 760150.”

If you need further information, please contact the coordinator:

TECHNIKON Forschungs- und Planungsgesellschaft mbH
Burgplatz 3a, 9500 Villach, AUSTRIA
Tel: +43 4242 233 55 Fax: +43 4242 233 55 77
E-Mail: coordination@epic-h2020.eu