The EPIC project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 760150.

EPIC

Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding

Next-Generation Channel Coding Towards Terabit/s Wireless Communications

Large challenges on the baseband processing in wireless communication are present, in particular in Channel coding (Forward Error Correction):

- Future Beyond-5G use cases expected to require wireless data rates in Terabit/s range, power envelope in the order of 1-10 watts
- The EPIC project aims to develop new Forward Error Correction (FEC) schemes for future Beyond-5G use cases targeting a throughput in the Tb/s range. **Focus will be on the most advanced FEC schemes: Turbo codes**, Low Density Parity Check **(LDPC) codes** and **Polar codes**
- Improvement from new silicon technology has to be complemented with improvements on the code level, the decoding algorithms and the architectural level

Targets

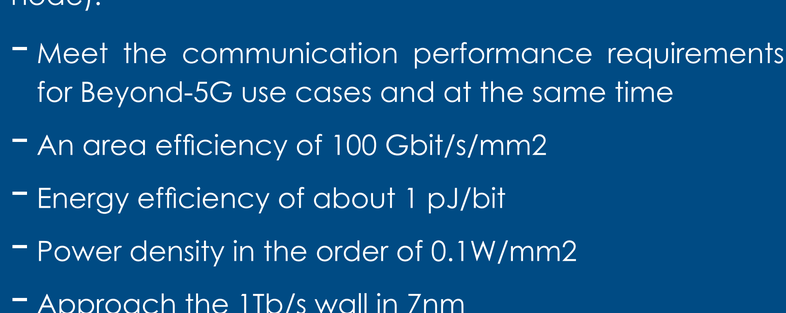
Targets fixed for the EPIC project (for 7nm technology node):

- Meet the communication performance requirements for Beyond-5G use cases and at the same time
- An area efficiency of 100 Gbit/s/mm2
- Energy efficiency of about 1 pJ/bit
- Power density in the order of 0.1W/mm2
- Approach the 1Tb/s wall in 7nm

Standardization

EPIC has attended the IEEE 802.15 THz IG Meeting, from the 7th to 8th of May, 2018 in Warsaw, Poland.

Upcoming standardization plan: EPIC plans to attend several more standardization activities.



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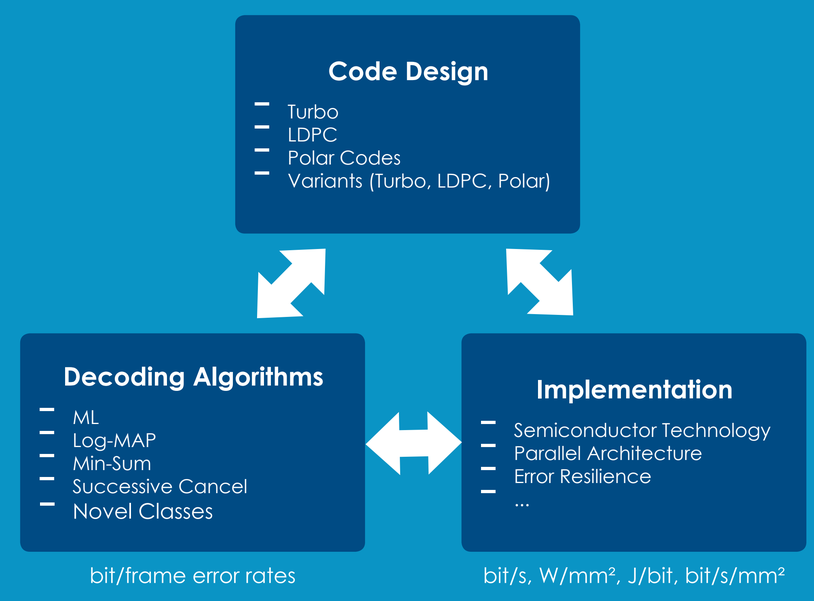
Holistic FEC Design

The biggest implementation challenge is achieving the requirements on energy efficiency and power density while maintaining communication performance and the necessary flexibility required by the use cases.

EPIC pursues a holistic approach in which information theory, code design, algorithms/ architecture co-design, front-end and back-end implementation optimization are considered together. Core step: Verification and ranking of FEC Algorithms.



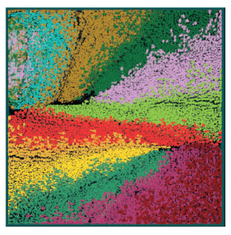
EPIC FEC Design Framework

High-Throughput Decoders

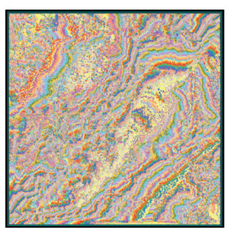
EPIC dataflow architectures allow very high throughput approaching the 1Tb/s wall in 7nm technology.
Most prominent techniques to achieve high-throughput on architectural level are spatial parallelism and functional parallelism (pipelining).

Pipelining:
Advantages: Large locality, compared to spatial parallelism.
Challenges: In pipelined architectures throughput is increased at the cost of additional storage since several blocks have to be kept simultaneously in the pipeline stages.

Deeply pipelined architectures can suffer from large storage requirements that are a major source of power consumption.
To achieve throughput far beyond 100 Gbit/s, dataflow and tree structures must be flattened, or "unrolled", and pipelined respectively.



Layout LDPC code decoder in 28nm Area is 2.8 mm². The different colors represent the different decoding iteration (in total 9 iterations)



Layout Polar decoder. Area is 4.3 mm². Code block 1024, Rate=0.5. Each color represents a stage in the factor tree traversal (in total 385 stages).

LDPC decoder supporting a 802.11ad standard code

- Synthesized on a 28nm Fully Depleted Silicon on Insulator (FD-SOI) technology under worst case Process, Voltage and Temperature (PVT) assumption
- Characterized for different voltages
- Extrapolating outcomes at these different voltages to 7nm gives a throughout of 480Gbit/s and 1.5pJ/bit

Polar code decoder

- Decoding is performed with the successive cancellation algorithm
- Synthesized on the same technology and under the same conditions as the LDPC decoder
- Extrapolating achieved numbers to the 7nm with a maximum frequency of 1Ghz results in an energy efficiency of less than 2 pJ/bit

Consortium: TECHNIKON, ERICSSON, TECHNISCHE UNIVERSITÄT KAISERSLAUTERN, CREONIC, POLARAN, INTERDIGITAL EUROPE, imec, IMT Atlantique Bretagne-Pays de la Loire École Mines-Télécom