The EPIC project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 760150.

EPIC

Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding

FEC Bottleneck in Beyond-5G Wireless Tb/s

Forward-Error-Correction (FEC) belongs to the most complex and computationally intense component in the baseband chain

3G → 4G → 5G baseband and FEC implementations heavily took advantage of progress in microelectronics driven by Moore's law: smaller area, lower power consumption, higher clock frequency

However, Moore's Law Slow-down:

- Power and power density will emerge as a binding constraint
- Clock frequency larger than 1 GHz will not be feasible due to power constraints, but at the same time increasing throughput requirements
- Power constraint combined with ever increasing throughput requirements → energy efficiency will be critical (J/bit)

Practical Wireless Tb/s FEC Requirements

- Meet the communication performance requirements for Beyond-5G use cases
- >1 Tb/s throughput (in 7nm)
- ~ 10 mm2 chip area for FEC IP block
- ~ 1 Watt Power envelope
- ~ 1 GHz clock frequency limit

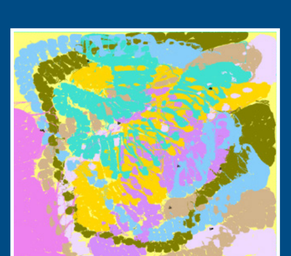
PRACTICAL B5G TBPS FEC KPI BOUNDS

Chip area limit	~ 10 mm^2
Area efficiency limit	~ 100 Gb/s/ mm^2
Energy efficiency limit	~ 1 pJ/bit
Power density limit	~ 0.1 W/mm^2

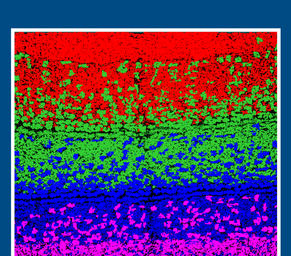
First EPIC High-Throughput Decoder Implementations

All designs in 28nm low Vt FDSOI technology, worst case PVT

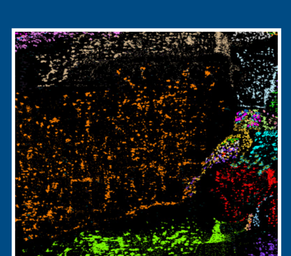
Code	Blocksize [bit]	Code rate	Frequency [MHz]	Throughput [1] [Gbit/s]	Area [mm^2]	Power [mW]	Area efficiency [Gbit/s/mm^2]	Energy efficiency [pJ/bit]
Turbo code (4 iter)	128	1/3	800	102	23.6	-	4.34	-
LDPC code (4 iter)	1200	4/5	400	480	2.79	3000	172	6.3
Polar code	1024	1/2	746	764	2.95	3300	259	4.4



102 Gbit/s Turbo decoder. The area is 23.61mm^2. Different colors represent the eight different MAP decoders originating from the four unrolled iterations (each iteration requires two MAP decoders).



480 Gbit/s LDPC decoder. The area is 2.79mm^2. Each color represents check and variable node functional units corresponding to one iteration (4 in total).



764 Gbit/s Polar decoder. The area is 2.95mm^2. Each color represents a pipeline stage (105 in total), memory is colored black

Holistic FEC Design

EPIC pursues a holistic approach: joint consideration of information theory, code design, algorithms/ architecture co-design, front/back-end

Code Design
- Turbo
- LDPC
- Polar Codes
- Variants (Turbo, LDPC, Polar)

Decoding Algorithms
- ML
- Log-MAP
- Min-Sum
- Successive Cancel
- Novel Classes

Implementation
- Semiconductor Technology
- Parallel Architecture
- Error Resilience
- ...

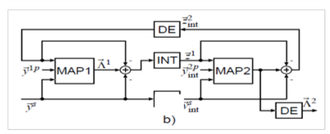
bit/frame error rates

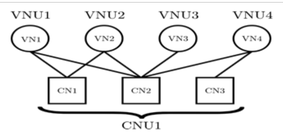
bit/s, W/mm^2, J/bit, bit/s/mm^2

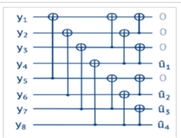
CHALLENGES
- Energy efficient high throughput architectures → large locality and regularity, large parallelism required
- But Information theory → irregularity, iterative

EPIC FEC Design Framework

Code	Decoding algorithms	Parallel vs. serial	Locality	Compute kernels	Transfers vs. compute
Turbo code	MAP	serial/iterative	low (interleaver)	Add-Compare-select	compute dominated
LDPC code	Belief propagation	parallel/iterative	low (Tanner graph)	Min-Sum/add	transfer dominated
Polar code	Successive cancelation/List	serial	high	Min-Sum/add/sorting	balanced



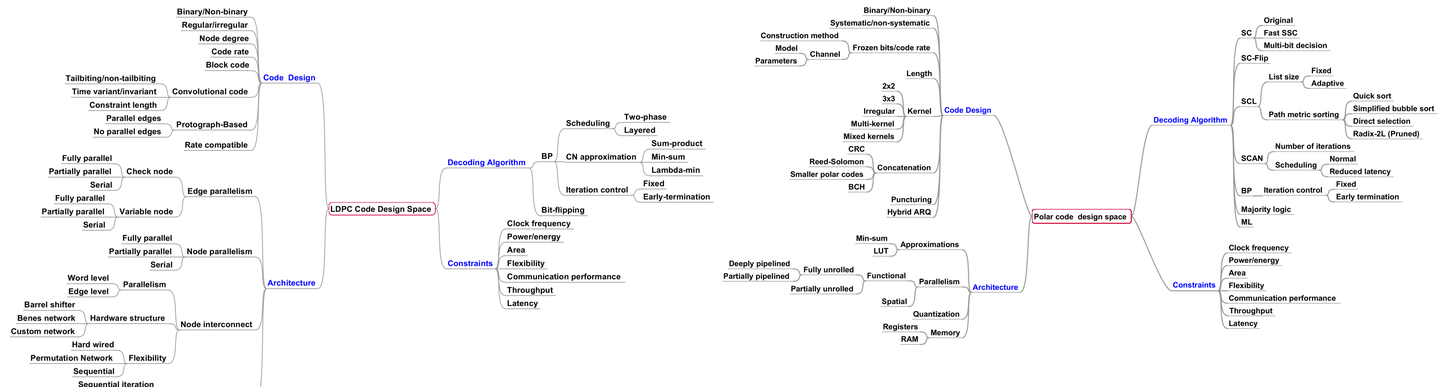




Key Methodology

Many Trade-Offs between code design, decoding algorithms, architecture, communications performance

- Set up design space for each code class containing all design para-meters → huge design space
- Design space exploration (DSE) to prune the design space under EPIC KPI constraints
- Select most promising candidates to derive new FEC solutions



Project Coordinator
MMag. Martina Truskaller
Technikon Forschungs- und Planungsgesellschaft mbH
Email: coordination@epic-h2020.eu Web: www.epic-h2020.eu

Technical Leader
Prof. Dr.-Ing. Norbert Wehn
Techische Universität Kaiserslautern
Email: wehn@eit.uni-kl.de

Consortium: TECHNIKON · ERICSSON · TECHNISCHE UNIVERSITÄT KAISERSLAUTERN · CREONIC · POLARAN · INTERDIGITAL EUROPE · imec · IMT Atlantique Bretagne-Pays de la Loire École Mines-Télécom