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EPIC Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding

Turbo Codes MWC2020

Major Contributions on Turbo Codes

- **First Fully Pipelined Turbo Decoder Hardware Architecture**
  - Flexible w.r.t. Frame Size & Code Rate, Virtual Silicon for 28nm technology
  - Throughput > 100Gb/s (factor 10 over SoA), Area Efficiency > 6 Gb/s/mm² (factor > 2 over SoA)
- **EPIC codes outperform LTE codes**
  - Gain of > 1dB esp. for high coding rates, short frames and low error rates
  - Maintain full rate compatibility down to the code bit
- **New Simplified Decoding Algorithm**
  - Complexity reduction of > 30% especially for high radix orders
  - No/Limited impact on error correcting performance

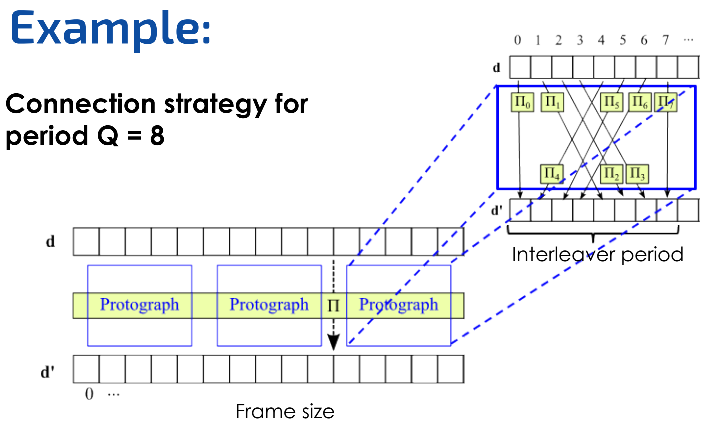
Puncturing Constrained Protograph Based Interleaving

- Interleaver is critical for error correcting performance and implementation complexity
- An efficient interleaver should respect a set of constraints (spread, cycle length, etc.)
- EPIC Approach: Periodic interleaver construction can give guarantees by design (verification of constraints within a single period vs. On whole frame size) [1]

Design Flow:

From target rate, Introduce additional puncturing
↓
Classify positions of a period in terms of error-prone level
↓
Protograph = periodic connection strategy: Most reliable to least reliable positions in all periods up to the frame size

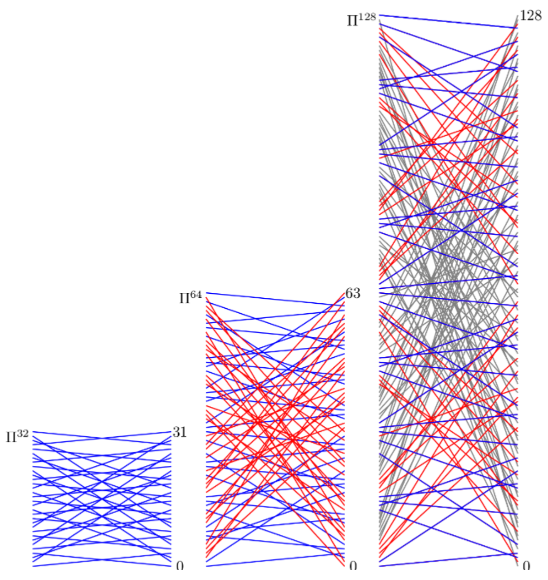
Example:



[1] R. Garzón-Bohórquez, C. Abdel Nour and C. Douillard, „Protograph-Based Interleavers for Punctured Turbo Codes," in IEEE Transactions on Communications, vol. 66, no. 5, pp. 1833-1844, May 2018. doi: 10.1109/TCOMM.2017.2783971

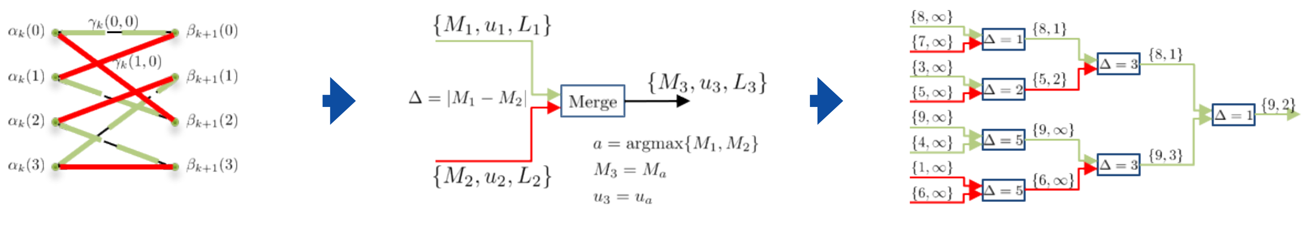
Code design: Flexible interleaving

- Design sets of interleavers with maximum overlapping to achieve frame
- For overlapping connections (blue), no multiplexing is required,
- For partial overlaps (red) multiplexers are smaller
- Interleaver set supporting frame sizes K ε {32,64,128}: $\pi(i) = \left(P \cdot \mathbf{S}_{i \bmod Q}\right) \bmod K$
- Interleaver sets are used in for the FF-UXMAP decoder [2]



New decoding algorithm: Local-SOVA

- For soft output calculation, use merge operation and update rules to find „winning" paths



- Computed LLRs are equivalent to those of the commonly used Max-Log-MAP algorithm
- High radices: Lower complexity than Max-Log-MAP. **Up to 27% reduction in computational complexity! [2]**

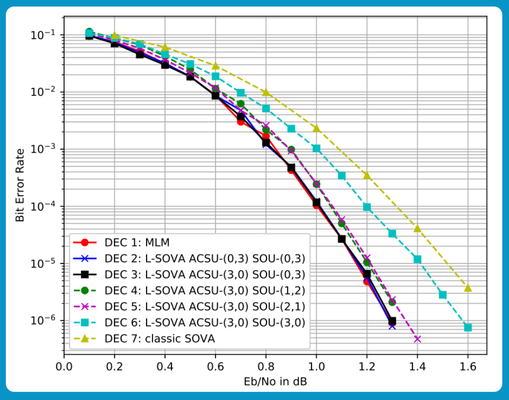
Schemes	$\mathcal{C}_{\mathrm{MLM}}$	$\mathcal{C}_{\mathrm{LSOVA}}$	$\frac{\mathcal{C}_{\mathrm{LSOVA}}}{\mathcal{C}_{\mathrm{MLM}}}$	$\frac{\mathcal{C}_{\mathrm{MLM}}}{\#\mathrm{bits}}$	$\frac{\mathcal{C}_{\mathrm{LSOVA}}}{\#\mathrm{bits}}$
Radix-2	79	77	0.975	79	77
Radix-4	206	151	0.733	103	75.5
Radix-8	493	361	0.732	164.3	120.3

[2] V. H. S. Le, C. A. Nour, E. Boutillon and C. Douillard, "Revisiting the Max-Log-Map algorithm with SOVA update rules: new simplifications for high-radix SISO decoders," in IEEE Transactions on Communications. doi: 10.1109/TCOMM.2020.2966723

Algorithm: Simplified Local-SOVA decoding

- Local-SOVA allows further simplifications for high radixes at minimal BER penalty
- Up to 38% reduction in computational complexity! [3]

Algorithm	Computational complexity	Complexity normalization	Performance loss at BER 10^{-6} (dB)
MLM	493	1	–
DEC 2	361	0.73	0.0
DEC 3	329	0.67	0.0
DEC 4	317	0.64	0.05
DEC 5	311	0.63	0.05
DEC 6	308	0.62	0.3

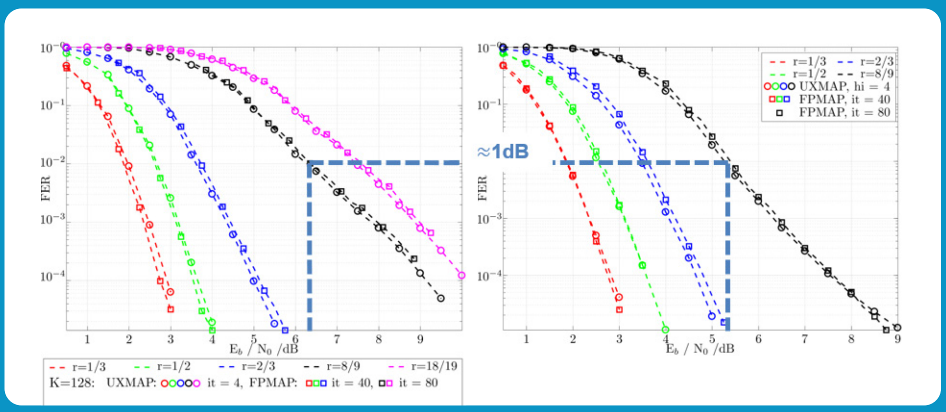


Architecture: UXMAP Decoder FER Performance

- EPIC Turbo Code: 1 dB superior compared to LTE code @ FER 10-2 Rate 8/9

- Comparison: UXMAP vs. FPMAP Decoder [3]:
- UXMAP requires a significantly lower number of decoding iterations (it)
- Low code rates: FPMAP: 40it – UXMAP: 4it for similar FER performance
- High code rates: FPMAP: 80it – UXMAP: 4it for similar performance

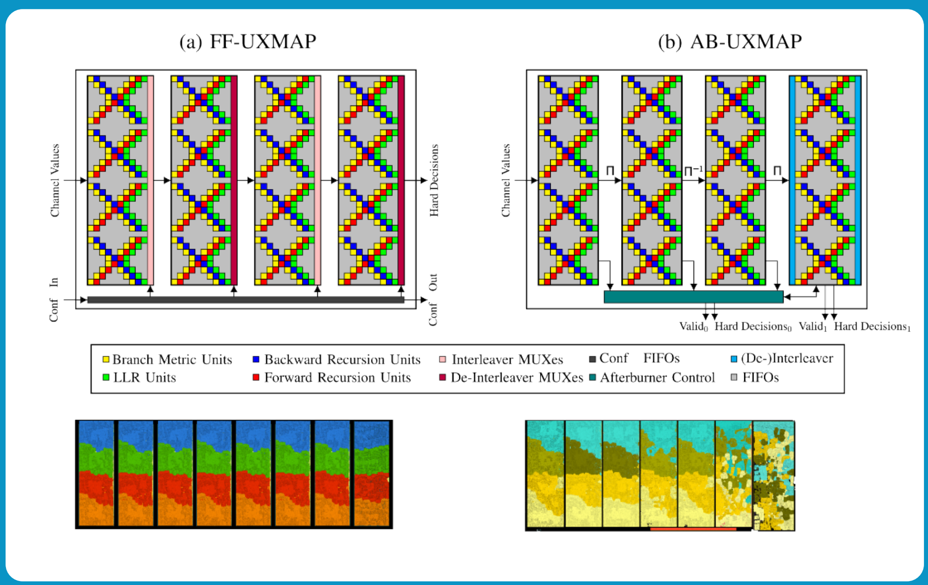
LTE, K=128, max-Log-MAP, BPSK, AWGN PPC, K=128, max-Log-MAP, BPSK, AWGN



[3] S. Weithoffer, C. A. Nour, N. Wehn, C. Douillard and C. Berrou, "25 Years of Turbo Codes: From Mb/s to beyond 100 Gb/s," 2018 IEEE 10th International Symposium on Turbo Codes & Iterative Information Processing (ISTC), Hong Kong, Hong Kong, 2018, pp. 1-6. doi: 10.1109/ISTC.2018.8625377

Architecture: Advanced UXMAP Implementations [4]

- 28 nm FD-SOI technology, worst-case PVT conditions
- Frame Flexible UXMAP (FF-UXMAP) with support for several frame sizes
- UXMAP with iterative Afterburner (AB-UXMAP) with increased area efficiency



Decoder Schematics and Layouts

Architecture	FF-UXMAP	AB-UXMAP
Codeblock Size [bit]	384/192/ 96	384
Iterations	4	3+4
Supported Code Rate	flexible	flexible
Frequency [MHz]	800	800
Throughput [Gb/s]	102.4	102.4
Core Area [mm²]	16.54	14.32
Area Eff. [Gb/s/mm²]	6.19	7.15

[4] Stefan Weithoffer, Oliver Griebel, Rami Klaimi, Charbel Abdel Nour, Norbert Wehn. Advanced Hardware Architectures for Turbo Code Decoding Beyond 100 Gb/s, accepted at WCNC 2020. 2019. (hal-02319732)

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