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EPIC **Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding**



LDPC Decoders

Information throughput of LDPC block decoder (BC)

$$T_{LDPC} = N \cdot R \cdot \frac{1}{I} \cdot P \cdot f \quad [\text{bit/s}]$$

N: Code block size
R: Code rate
I: Number of decoding iterations
f: Clock frequency

$$\text{Decoding parallelism } P = \frac{\text{number of Tanner graph edges processed per clock cycle}}{\text{total number of Tanner graph edges}}$$

$f \sim 1\text{GHz}$, $T_{LDPC} \sim 1\text{Tb/s}$ in 7nm technology node

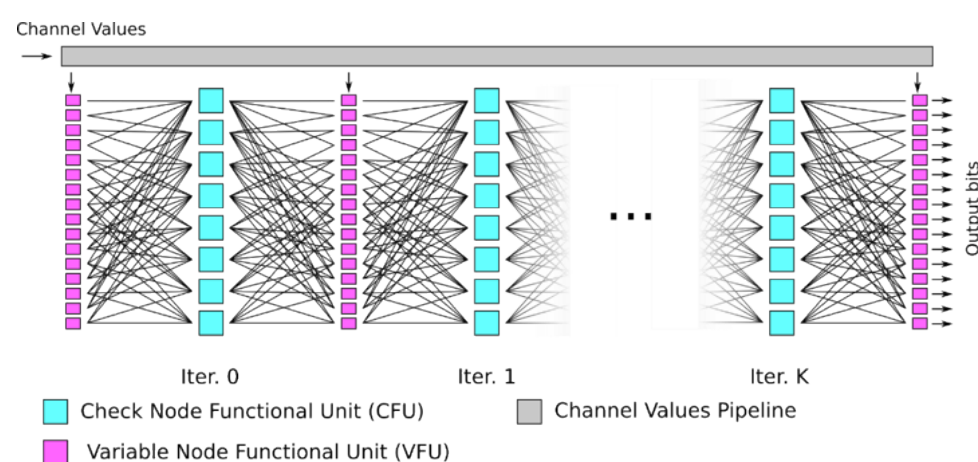
- > 1000 bits have to be decoded in single clock cycle => block level parallelism mandatory
- $P=I$ => pipelining (unrolling) of iterations mandatory
- LDPC-BC decoder for $N \sim 1000$ bits

Block sizes $\gg 1000$ bits

- SC-LDPC code with submatrix size ~ 1000 bits
- SC-LDPC Architecture: window decoder with unrolled iterations alike LDPC block decoder

LDPC-BC Decoding Architecture

- Block level parallel LDPC decoder architecture with pipelined (unrolled) iterations [1]
- Processes multiple code blocks in the decoder pipeline and outputs one code block every clock cycle
- Number of iterations determines the pipeline length



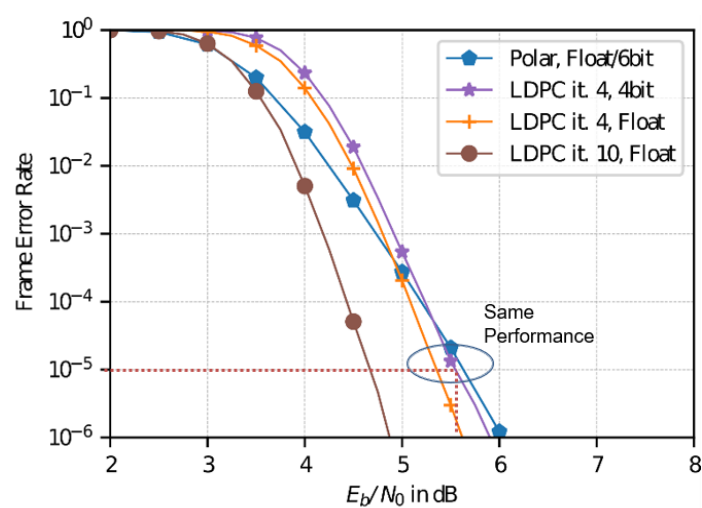
[1] C. Kestel, M. Herrmann, N. Wehn, "When Channel Coding Hits the Implementation Wall", IEEE 10th Int. Symposium on Turbo Codes & Iterative Information Processing (ITC), pp. 1-6, 2018.

LDPC-BC: Communications Performance

- EPIC LDPC code: 4x24 protograph with lifting factor $Z = 43$ ($N = 1032$ and rate $R = 5/6$)
- Decoding algorithm: Min-Sum (two-phase/flooding scheduling)

Comparison: LDPC Code versus Polar Codes

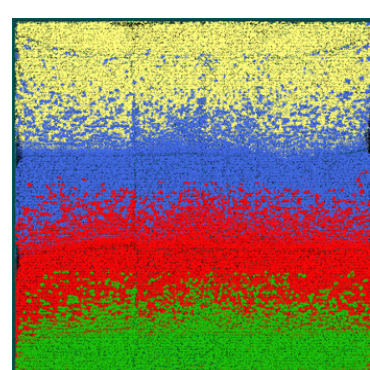
- LDPC decoder requires 4 iterations and 4 bit quantization to meet the performance of the EPIC Polar decoder @ FER=10⁻⁵
- EPIC Polar decoder: density evolution, similar length and rate as LDPC, successive cancellation decoding



Performance comparison of EPIC LDPC and Polar decoders

LDPC-BC Decoder Implementation Results

- 28nm FD-SOI technology, worst-case PVT conditions
- Comparison: EPIC SC Polar decoder based on pipelined (unrolled) Polar factor tree traversal
- Both decoders targeted frequency of 400 MHz in 28nm technology



Layout LDPC decoder

- iteration 4
- iteration 3
- iteration 2
- iteration 1

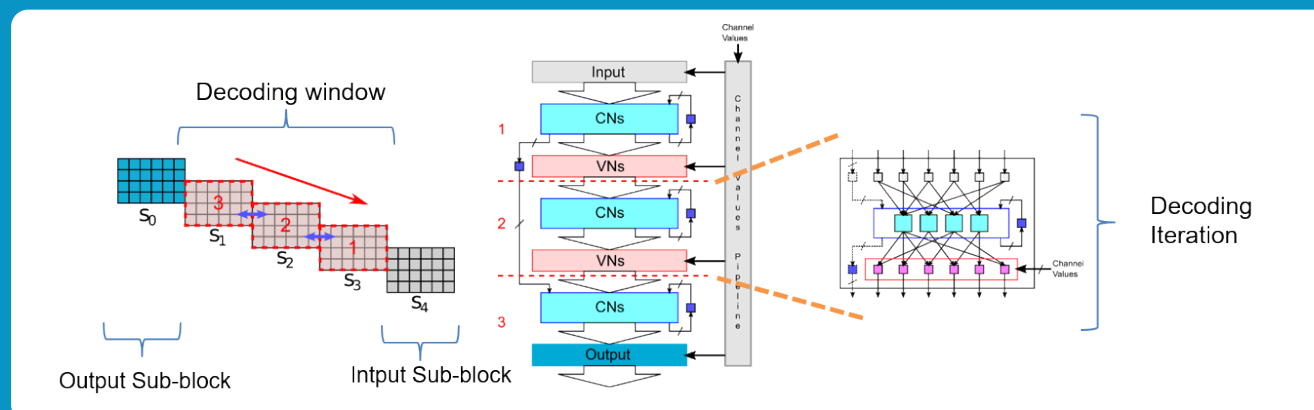
Architecture	LDPC	Polar
Codeblock Size [bit]	1032	1024
Iterations	4	-
Frequency [MHz]	347	400
Latency [ns]	40.3	82.5
Throughput [Gb/s]	358.5	411
Core Area [mm ²]	2.33	1.67
Power [W]	2.37	1.13
Energy Eff. [pJ/bit]	6.62	2.75
Area Eff. [Gb/s/mm ²]	154	246

LDPC MWC2020

SC-LDPC Decoding Architecture

Fully parallel window decoder architecture with pipelined (unrolled) iterations for spatially coupled LDPC and LDPC convolutional codes based on [1]

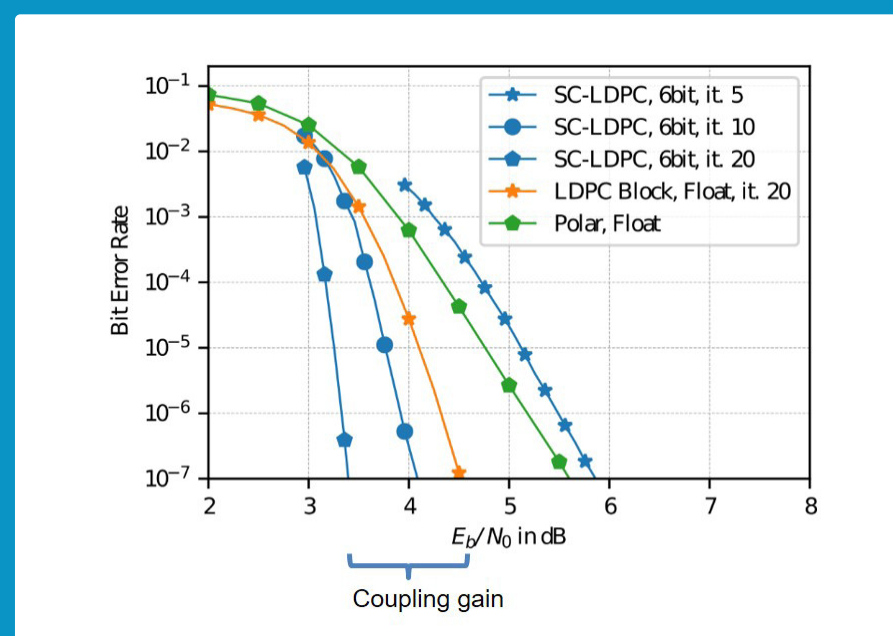
- Supports arbitrary block sizes, strong improved waterfall region and lower error floor compared to LDPC-BC
- Reduced latency compared to conventional window decoder with negligible loss in performance
- Processes multiple sub-matrices in parallel and outputs one sub-block every clock cycle



[1] N. U. Hassan, M. Schlüter and G. P. Fettweis, "Fully parallel window decoder architecture for spatially-coupled LDPC codes", 2016 IEEE Int. Conf. on Communications (ICC), 2016.

SC-LDPC Communications Performance

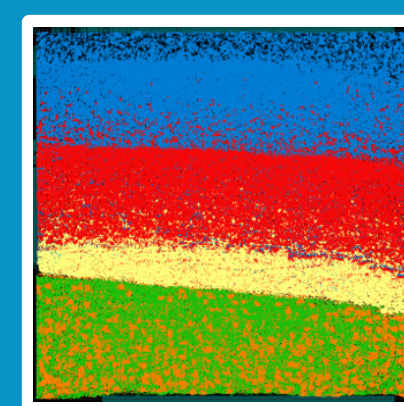
- EPIC SC-LDPC code: Sub-matrix size 512 x 1280, 80 sub-matrices in one block => $N \sim 100.000$, $R = 4/5$
- Decoding algorithm: unrolled window with Min-Sum (two-phase/flooding scheduling)
- For comparison: performance of the aforementioned EPIC LDPC-BC and Polar codes ($N \sim 1000$, $R = 5/6$) with Min-Sum and SC decoding



SC-LDPC Decoder Implementation Results

First known implementation of this new SC-LDPC decoder architecture

- 22nm FD-SOI technology, worst-case PVT conditions
- 512 Gb/s coded throughput (410 Gb/s info throughput @ Rate $R=4/5$)



Layout SC-LDPC decoder

- decoder 4
- decoder 2
- decoder 0
- decoder 1
- decoder 3

Parameter	Value
Window Size [bit]	5x1280
Iterations	5
Frequency [MHz]	400
Latency [ns]	30.0
Coded Throughput [Gb/s]	512
Core Area [mm ²]	3.94
Power [W]	3.13
Energy Eff. [pJ/bit]	6.11
Area Eff. [Gb/s/mm ²]	130

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