High-Throughput Polar Code IP Cores for FPGAs

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***Abstract*—This demo presents polar code implementations that reach 100 Gb/s on FPGAs with a coding gain of more than 6dB at BER 10^{-12}.**

I. Introduction

Two IP core products are demonstrated in an end-to-end configuration on a Xilinx Ultrascale+ (16nm) Virtex FPGA demo board. The first IP core implements a 100 Gb/s polar coding system using successive cancellation decoder. The second core implements a 50 Gb/s polar coding system using a list-of-two successive cancellation decoder. Potential use-cases for the IP cores are fiber-optic communications, C-RAN/V-RAN fronthauling, backhauling, data centers, virtual/augmented reality, chip-to-chip and intra-chip communications, and data kiosks.

The overview of the demo is shown in Fig. 1. Demo type (IP core) and other demo parameters such as number of trials, the Eb/No range, etc. are selected on a PC using a GUI and the corresponding configuration file is uploaded to the FGPA through a JTAG cable. The demo uses BPSK modulation and an AWGN channel model. The throughput, bit error rate (BER) and frame error (FER) figures, and latency are displayed on the PC screen in real-time as the simulation takes place on the FPGA.

II. Demo 1

Demo 1 illustrates a polar coding system with successive cancellation decoder. Code block length is 1024 and code rate is 854/1024 (20% overhead).

A. Key Performance Indicators

- Clock frequency 125 MHz
- Throughput > 100 Gb/s
- Power consumption: 5mW encoder, 391mW decoder
- Latency less than 1 µs

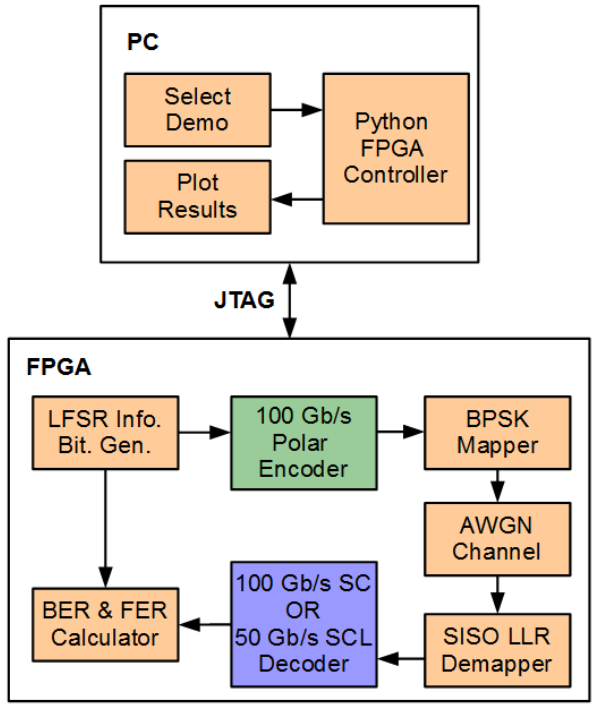

Figure 1: Demo block diagram

B. Resource Usage

The FGPA resources consumed by the encoder and decoder in Demo 1 are shown in the following table. (Percentages indicate the resources consumed as a fraction of total resources.)

	LUT	**FF**	**BRAM (36 Kbit)**
Encoder	1,842 (0.14%)	1,825 (0.07%)	-
Decoder	53,247 (4.08%)	35,192 (1.35%)	136 (6.75%)

C. Performance

The BER/FER performance of the polar coding system in Demo 1 is shown in Fig. 2. The dashed lines show the floating-point performance using software simulation. Implementation loss is 0.28 dB at 10^{-6} BER

relative to software simulation. A coding gain of 6.21 dB is attained at 10^{-12} BER relative to the uncoded transmission.

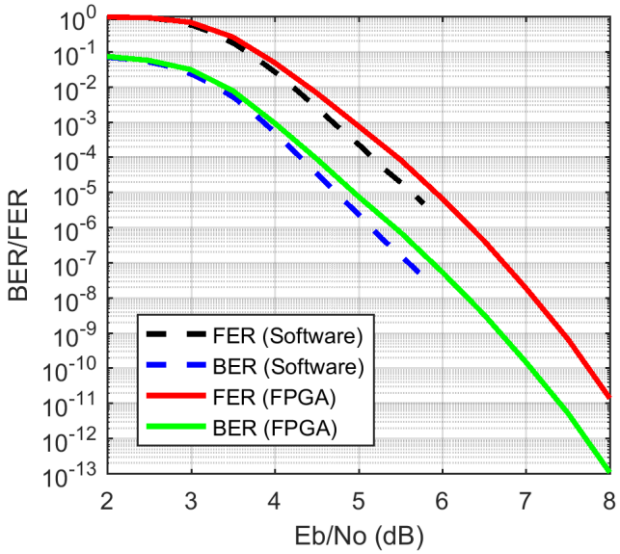

Figure 2: Performance of 100 Gb/s SC(1024,854)

III. Demo 2

Demo 2 illustrates an FPGA-based polar coding system using cyclic redundancy check (CRC)-aided successive cancellation list decoder with list size 2 and CRC length 4. The block length is 1024 and code rate is 888/1024 (15% overhead).

A. *Key Performance Indicators*

- FPGA clock frequency 65 MHz
- Throughput > 50 Gb/s
- Power consumption: 4mW encoder, 568mW decoder
- Latency less than 1 µs

B. *Resource Usage*

The FGPA resources consumed by the encoder and decoder in Demo 1 are shown in the following table. (Percentages indicate the resources consumed as a fraction of total resources.)

	LUT	**FF**	**BRAM (36 Kbit)**
Encoder	1,884 (0.16%)	1,918 (0.08%)	-
Decoder	190,084 (16.08%)	63,528 (2.69%)	108 (4.98%)

C. *Performance*

The BER/FER performance of the polar coding system in Demo 2 is shown in Fig. 3. The dashed lines show the floating-point performance using software simulation. Implementation loss is 0.05 dB at 10^{-6} BER relative to software simulation. A coding gain of 7.3 dB is attained at 10^{-12} BER relative to the uncoded transmission.

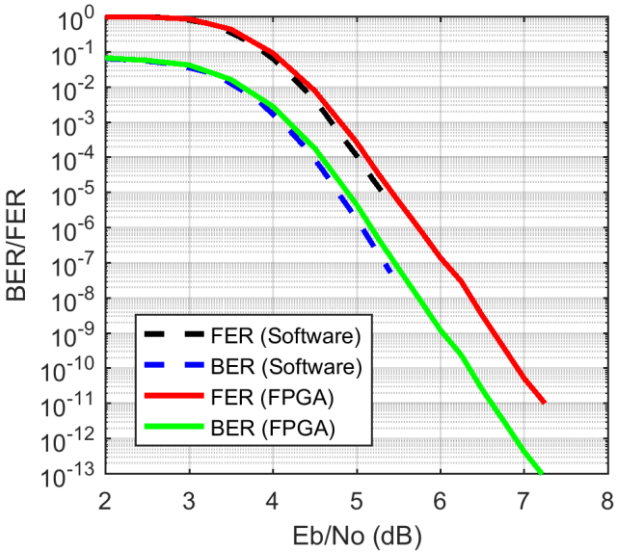

Figure 3: Performance of 50 Gb/s SCL(1024,888)

IV. ASIC IP Cores

ASIC versions of the polar encoder/decoder IP cores in the above demos are under development in the H2020 EPIC project. Target implementation parameters at 16nm technology are 1 Tb/s throughput, 1 pJ/b energy efficiency, and 100 Gb/s/mm^2 area efficiency.

Acknowledgement

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POLARAN LTD (www.polaran.com) offers a full range of polar code IP cores for FPGAs and ASICs. For further information and product inquiries, please contact Polaran at info@polaran.com or call +90-312-2650224.