50 Gb/s Polar Code IP Core FGPA Demonstrator

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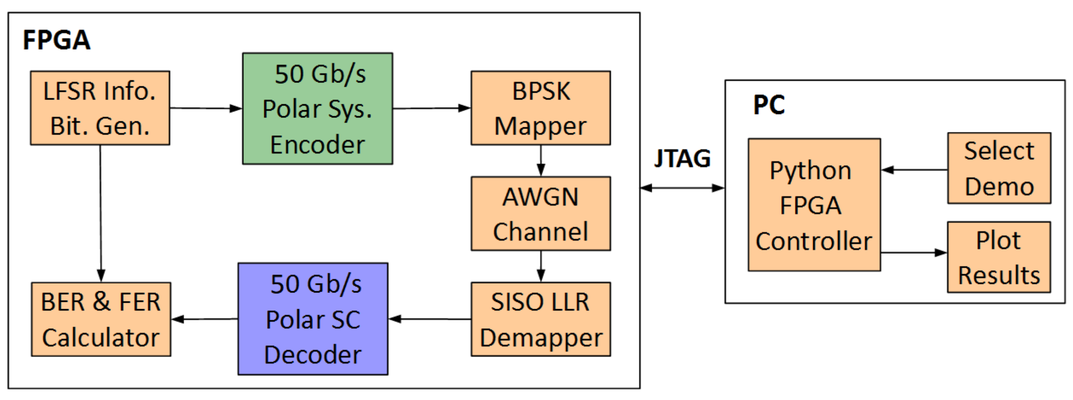
Introduction

This demo presents a length-1024 polar code implementation that reach 50 Gb/s on FPGAs with a coding gain of more than 7dB at 10^{-13} BER relative to uncoded transmission. Polar encoder and decoder IP core products are demonstrated in an end-to-end configuration on a Xilinx Ultrascale+ (16nm) Virtex FPGA demo board. The IP cores implement a 50 Gb/s polar coding system using systematic encoder and list-of-two successive cancellation (SCL) decoder aided with 4 bits CRC. Potential use-case for the IP core is fiber-optic communications, C-RAN/V-RAN fronthauling, backhauling, data centers, virtual/augmented reality, chip-to-chip, and intra-chip communications and data kiosks [1]. The ASIC version of the same IP core achieve 500 Gb/s data rates using a 16nm technology node.

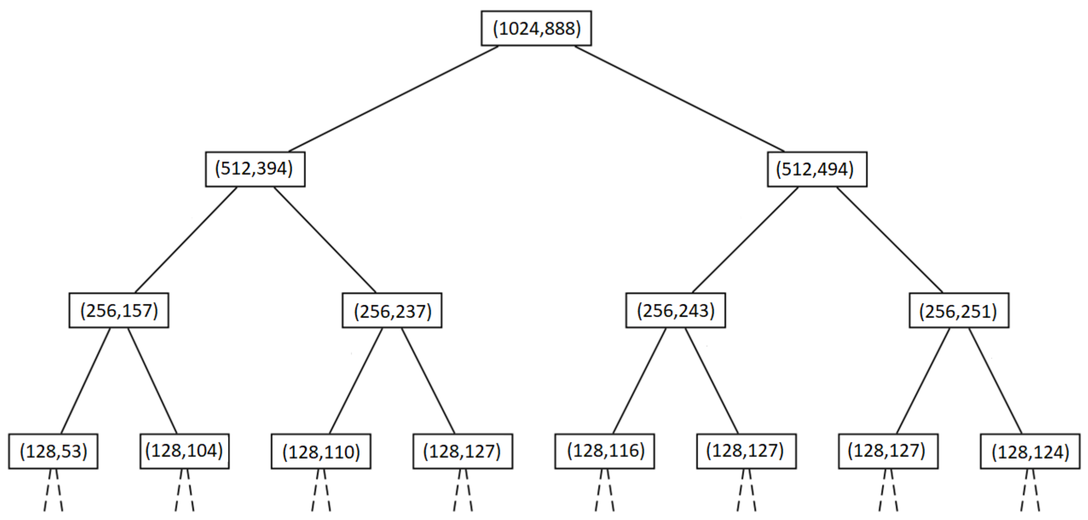
Demo Overview

The 50 Gb/s polar code IP core FPGA demonstration starts with the demo selection. Then, the selected bit file is uploaded to FPGA through the JTAG connection. The FPGA test starts with the random information bit generation and ends with bit error rate (BER) and frame error rate (FER) calculation. In this demo, 50 Gb/s polar systematic encoder and polar list-of-two successive cancellation (SCL) decoder are used. The throughput, BER/FER figures, and latency are displayed on the PC screen in real-time as the simulation takes place on the FPGA.



Decoding Algorithm

As an energy-efficient and high throughput FEC solution, we use a systematic polar code [2] with an enhanced list-of-two SC decoding algorithm. Algorithm follows the given decoding tree:

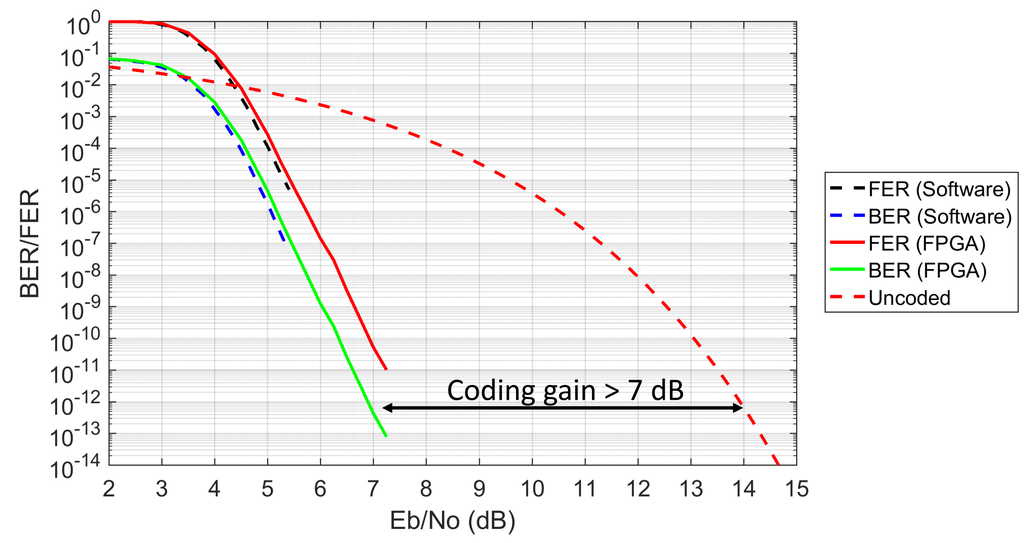


Decoder Architecture

We use an unrolled and deeply pipelined list-of-two SC decoder aided with CRC architecture with fully-parallel processing units. The unrolled architecture utilizes a dedicated logic block for each set of operation.

Performance Results

The simulations have been carried out over an AWGN channel with BPSK modulation of the (1024,888) list-of-two SC polar decoder aided with CRC on FPGA. Compared to the uncoded transmission, coding gain of the decoder is more than 7dB at 10^{-13} BER.

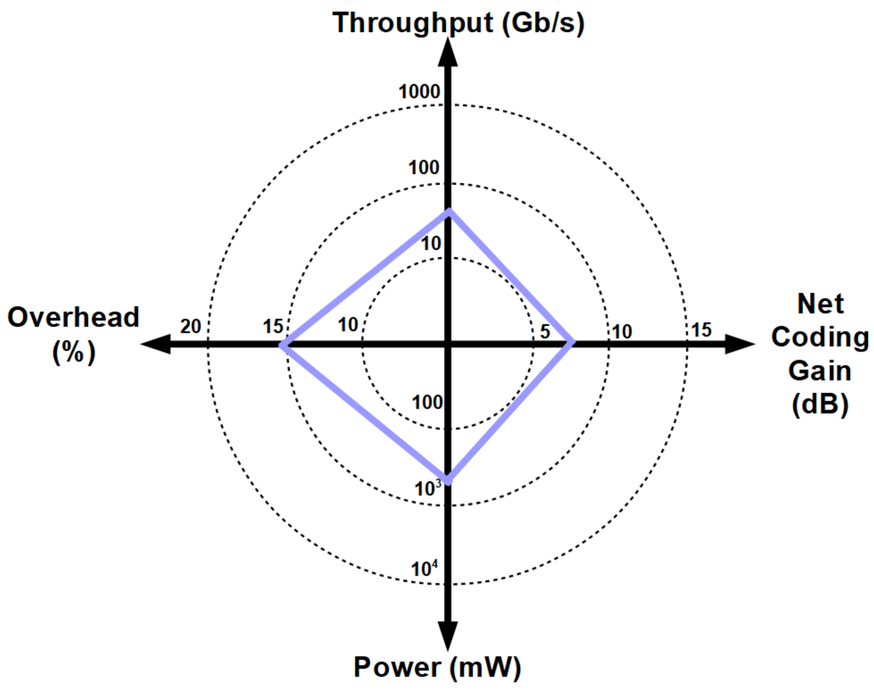


FPGA Implementation Results

The (*N*=1024, *K*=888) polar encoder and decoder IP cores are implemented on Xilinx Virtex-7 Ultrascale+ FPGA. The clock frequency is **65 MHz** and the net throughput is **57.7 Gb/s** for both encoder and decoder IP cores. In order to reduce the utilization of the LUTRAM resources, the decoder uses the dedicated 36K BRAM resources of the target FPGA.

(Percentages indicate the resources comsumed as a fraction of total resources.)

Name	LUT	FF	BRAM	Latency	Power
Encoder	1,884 (0.16%)	1918 (0.08%)	-	2 CCs 31 ns	4 mW
Decoder	190,084 (16.08%)	63,528 (2.69%)	108 (4,98%)	65 CCs 1000 ns	568 mW



Conclusion

We demonstrate an end-to-end system of list-of-two SC decoder. System operates at 65 MHz clock frequency on FPGA. The FPGA implementation results show that the decoder IP Core exceeds 50 Gb/s throughput under 9.84 pJ/b energy efficiency with a coding gain of more than 7dB at 10^{-13} BER relative to uncoded transmission.

Acknowledgment

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Polaran Ltd. (**www.polaran.com**) offers a full range of polar code IP cores for FPGAs and ASICs. For further information and product inquiries, please contact Polaran at **info@polaran.com** or call **+90-312-2650224**

References

[1] M. Li, A. Bourdoux, *et. al.* "B5G wireless Tb/s FEC KPI requirement and technology gap Analysis," [Online]. Available: https://epic-h2020.eu/downloads/EPIC-D1.2-B5G-Wireless-Tbs-FEC-KPI-Requirement-and-Technology-Gap-Analysis-PU-M07.pdf, accessed June 11, 2019.

[2] E. Arıkan, "Systematic polar coding," *IEEE Comm. Lett.,* vol. 15, no. 8, pp.860-862, 2011.