100 Gb/s Polar Code IP Cores FGPA Demonstrator

Polaran Ltd.

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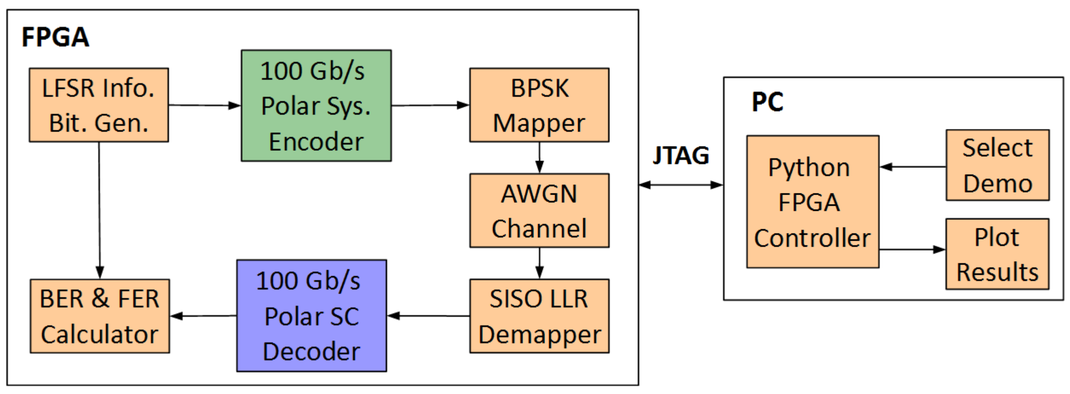
Introduction

This demo presents a length-1024 polar code implementation that reach 100 Gb/s on FPGAs with a coding gain of more than 6dB at 10^{-13} BER relative to uncoded transmission. Polar encoder and decoder IP core products are demonstrated in an end-to-end configuration on a Xilinx Ultrascale+ (16nm) Virtex FPGA demo board. The IP cores implement a 100 Gb/s polar coding system using systematic encoder and successive cancellation (SC) decoder. Potential use-cases for the IP cores are fiber-optic communications, C-RAN/V-RAN fronthauling, backhauling, data centers, virtual/augmented reality, chip-to-chip, and intra-chip communications and data kiosks [1]. The ASIC versions of the same IP cores achieve 1 Tb/s and 500 Gb/s data rates, respectively, using a 16nm technology node.

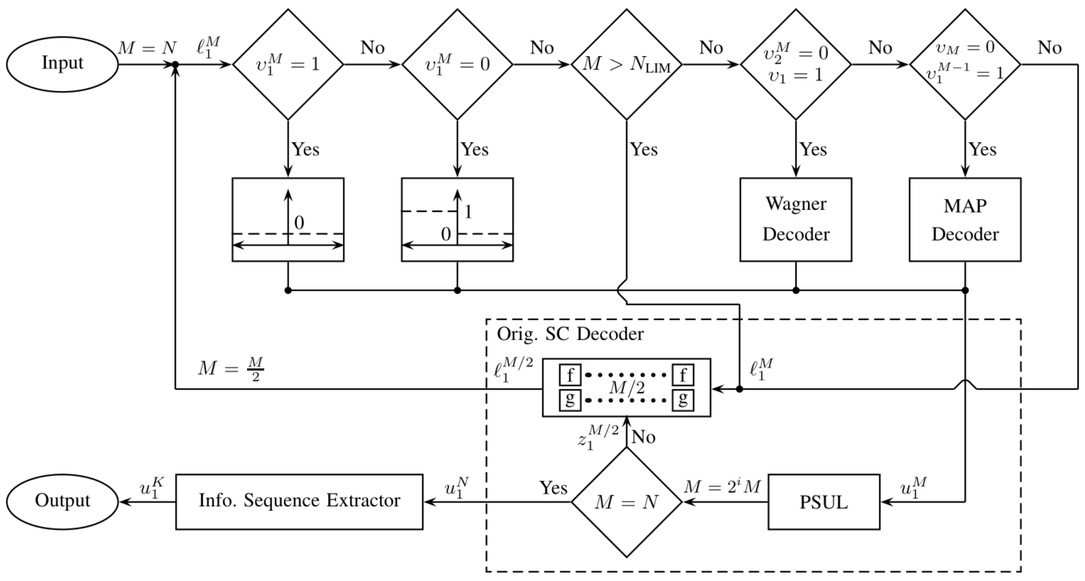
Demo Overview

The 100 Gb/s polar code IP core FPGA demonstration starts with the demo selection. Then, the selected bit file is uploaded to FPGA through the JTAG connection. The FPGA test starts with the random information bit generation and ends with bit error rate (BER) and frame error rate (FER) calculation. In this demo, 100 Gb/s polar systematic encoder and polar successive cancellation (SC) decoder are used. The throughput, BER/FER figures, and latency are displayed on the PC screen in real-time as the simulation takes place on the FPGA.

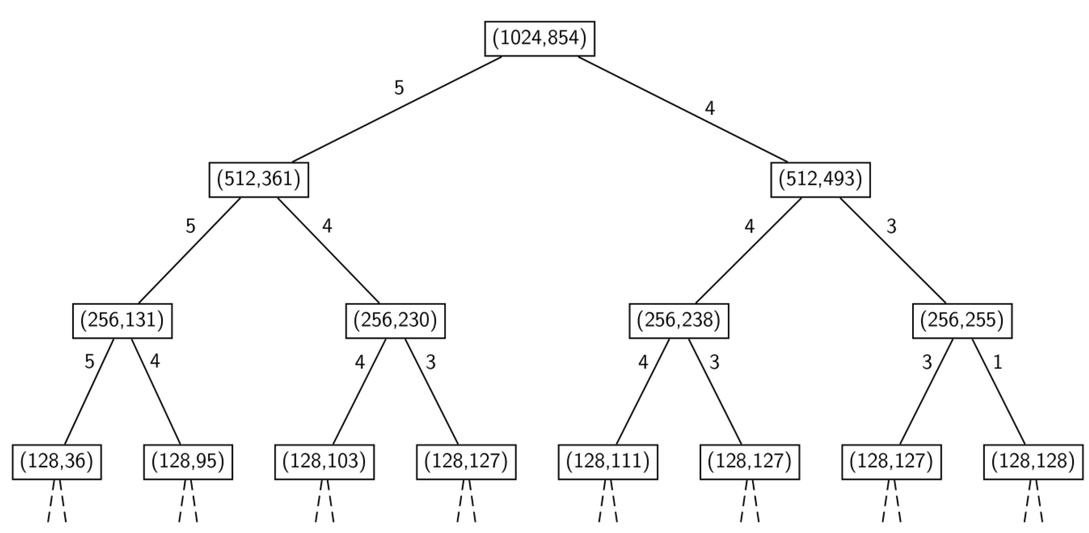


Decoding Algorithm

As an energy-efficient and high throughput FEC solution, we use a systematic polar code [2] with an enhanced SC decoding algorithm [3]. The algorithm exploits the low complexity Wagner and MAP decoders for speedup.

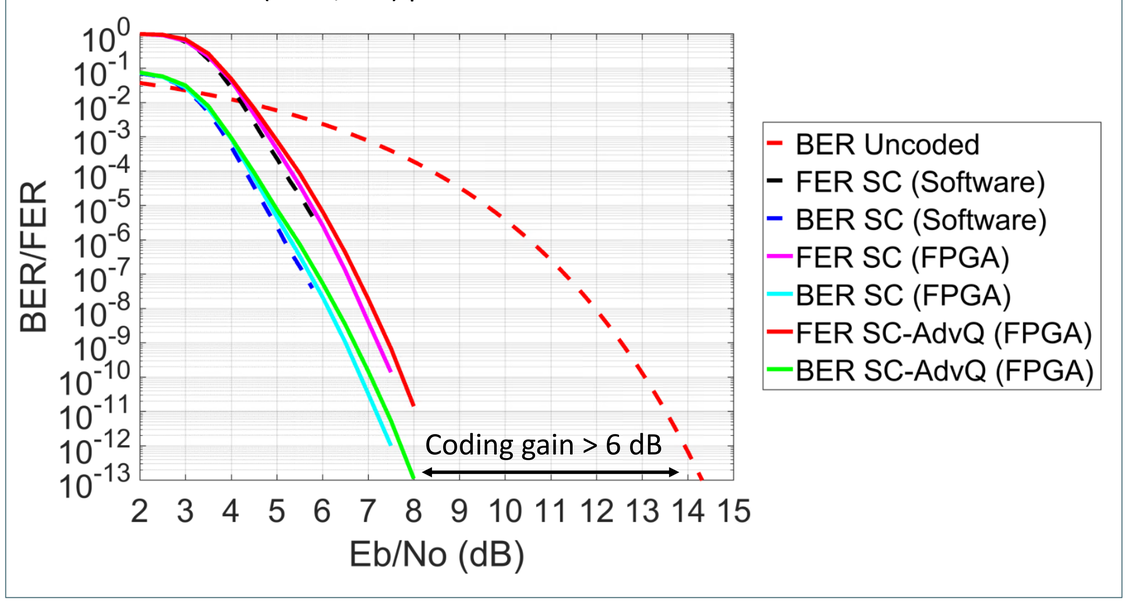


In order to reduce the computation complexity and memory of the SC algorithm, an adaptive quantization scheme is developed within 1-5 bits range of internal log-likelihood ratios (LLRs). The bit allocation is based on maximizing the mutual information between the input and output LLRs for each constituent polar code. For (*N*=1024, *K*=854) polar code, the adaptive quantization levels are given on the connectors between the constituent polar codes.



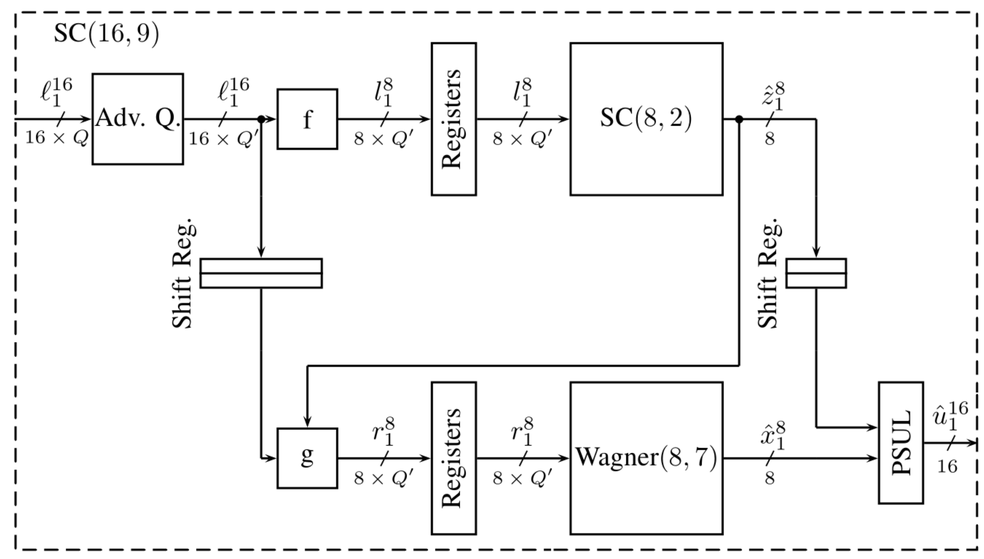
Performance Results

The simulations have been carried out over an AWGN channel with BPSK modulation of the (1024,854) polar code on FPGA.



Decoder Architecture

We propose an unrolled and deeply pipelined SC decoder architecture with fully-parallel processing units. The unrolled architecture utilizes a dedicated logic block for each set of operation. For example, the SC(16,9) decoder consists of the SC(8,2) and Wagner(8,7) sub-decoders. The consecutive pipelined decoding stages are merged by removing FFs for register balancing and timing in order to reduce the pipeline depth.



FPGA Implementation Results

The (*N*=1024, *K*=854) polar encoder and decoder IP cores are implemented on Xilinx Virtex-7 Ultrascale+ FPGA. The clock frequency is 125 MHz and the net throughput is 106.75 Gb/s for both encoder and decoder IP cores. In order to reduce the utilization of the LUTRAM resources, the decoder uses the dedicated 36K BRAM resources of the target FPGA.

Name	LUT	FF	BRAM	Latency	Power
Encoder	1,842 (0.14%)	1,825 (0.07%)	-	2 CCs 16 ns	5 mW
Decoder	53,247 (4.08%)	35,192 (1.35%)	136 (6,75%)	59 CCs 472 ns	391 mW

Conclusion

In order to reach 100 Gb/s net throughput within the physical limits of current FPGA technology, we demonstrate SC decoding algorithm with adaptive quantization levels. The decoder architecture is unrolled and deeply-pipelined with register-balancing. The FPGA implementation results show that the decoder IP Core exceeds 100 Gb/s throughput under 3.66 pJ/b energy efficiency with a coding gain of more than 6dB at 10^{-13} BER relative to uncoded transmission.

Acknowledgment

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Contact

Altuğ Süral
Design Engineer
Polaran Ltd. (**www.polaran.com**) offers a full range of polar code IP cores for FPGAs and ASICs. For further information and product inquiries, please contact Polaran at **info@polaran.com** or call **+90-312-2650224**.

References

[1] M. Li, A. Bourdoux, *et. al.* "B5G wireless Tb/s FEC KPI requirement and technology gap Analysis," [Online]. Available: https://epic-h2020.eu/downloads/EPIC-D1.2-B5G-Wireless-Tbs-FEC-KPI-Requirement-and-Technology-Gap-Analysis-PU-M07.pdf, accessed June 11, 2019.

[2] E. Arıkan, "Systematic polar coding," *IEEE Comm. Lett.*, vol. 15, no. 8, pp.860-862, 2011.

[3] E. Arıkan, "Channel polarization: a method for constructing capacity-achieving codes for symmetric binary-input memoryless channels," *IEEE Trans. Inform. Theory*, vol. 55, pp. 3051–3073, Jul. 2009.

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