# Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding

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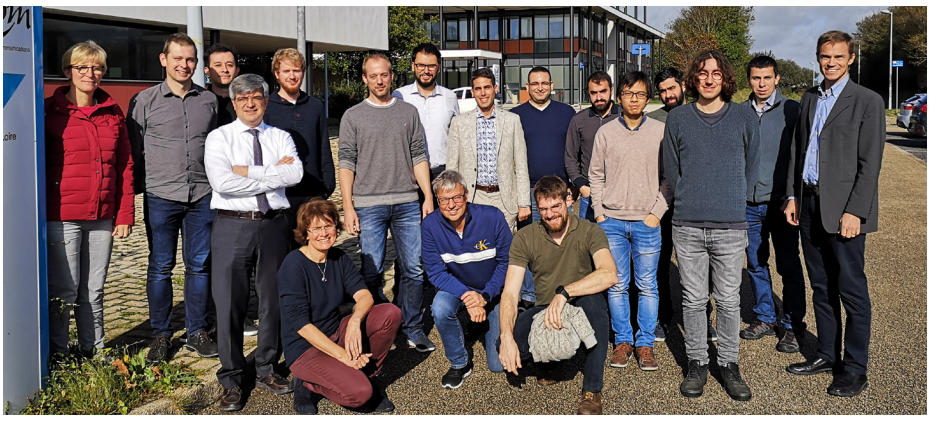
**Consortium**
8 partners (7 countries)

**Project Coordinator**
MMag. Martina Truskaller
coordination@epic-h2020.eu

Project number: **760150**
Project website:
**www.epic-h2020.eu**
Project start: **1st September, 2017**
Duration: **36 months**
Total cost: **EUR 2,966,268.75**
EC contribution: **EUR 2,966,268.75**


## Message from the Coordinator

The EPIC project is working hard to successfully finalize the ongoing work during the final project period. There have been numerous events and achievements since the last issue of the EPIC newsletter. The project partners participated in various workshops, meetings and conferences dedicated to the dissemination of EPIC, as well as to support progress of the project. One of the main events was the technical meeting in Brest in October 2019. The meeting has shown that EPIC made significant progress and the focus of the last project months is to finalize all the ongoing work and disseminate the results in the correspond communities.



## Technical Meeting Brest

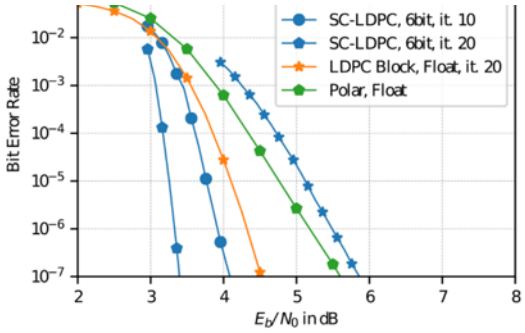
On the 9th and 10th of October 2019, the EPIC team converged for a technical meeting in Brest, France at partner IMT Atlantique. The aim of this meeting was to discuss technical progress, results, challenges as well as next steps of the project. Discussions included ongoing activities and tasks for the B5G FEC design and the prototyping/virtual hardware design. Several technical presentations on newest promising results as well as discussions about the methodology for fair comparison of the 3 different code types Turbo, LDPC and POLAR codes took place. Partners focused also on the upcoming dissemination/ communication activities. The technical meeting has shown that EPIC made large strides in the last months and the focus for the rest of the project is to finalize all the ongoing work and disseminate the results in the correspond communities.

## Achievements and work progress

Partners continued to enrich their respective simulation chains with additional technical contributions and started the evaluation of the different proposals for each code family. Following the mid-term review recommendations, regarding choices for frame sizes and coding rates that can be used to identify some scenarios for comparisons. Initial potential frame sizes and coding rates starting to emerge for each code family depending on the complexity of the currently developed hardware solutions. Necessary feedback regarding communications performance for the 3 code families was provided that helped select the final decoding algorithms to be implemented. Moreover, initial conditions for comparisons were agreed upon, setting a target for simulation results for the next months.

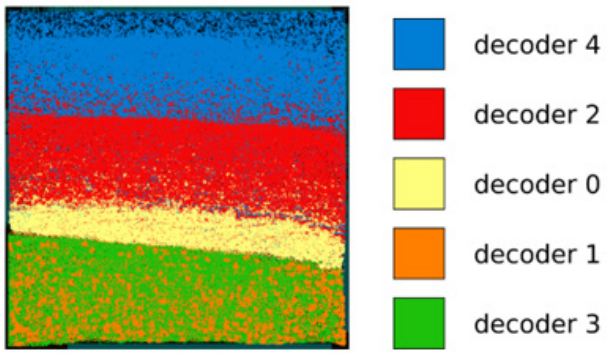
EPIC investigates different types of **LDPC decoders** for Tb/s throughput: LDPC block code (LDPC-BC) decoder for block sizes in the range from 1K to 10K and spatial coupled LDPC (SC-LDPC) decoders for very large block.
Two architectures for LDPC-BC were recently implemented in advanced technology nodes: a fully unrolled monolithic decoder in 28nm FDSOI technology and a frame-interleaved multi-core decoder in 16nm FINFET technology. The frame-interleaved architecture has a lower energy and area efficiency than the unrolled architecture but it provides larger flexibility. So, we can trade-off flexibility and implementation efficiency dependent on application requirements. Both decoders are based on the EPIC LDPC codes.
For larger block sizes EPIC investigates SC-LDPC decoders with submatrix sizes in the order of 1K. Advantages of SC-LDPC decoders are the support of arbitrary block sizes, strong improved waterfall region and lower error floor compared to LDPC-BC. To achieve highest throughput, we implemented for the first time a fully parallel window decoder with unrolled iterations alike the LDPC-BC unrolled decoder. This new architecture reduces the latency compared to conventional window decoder with negligible loss in performance. Is it to the best of our knowledge the first implementation of this type of architectures. The decoder was implemented in 22nm FDSOI technology.

The following graph shows the communication performance of the SC-LPDC in comparison to an LDPC-BC and Polar code for different number of iterations.




- EPIC SC-LDPC code: Sub-matrix size 512 x 1280, 80 sub-matrices in one block => N = ~100.000, R = 4/5
- Decoding algorithm: unrolled window with Min-Sum (two-phase/flooding scheduling)
- For comparison: performance of the EPIC LDPC-BC and Polar codes (N = ~1000, R= 5/6 with Min-Sum and SC decoding

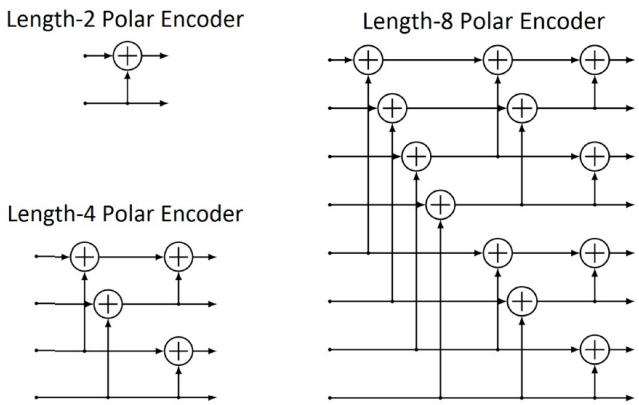
Below you see the layout and achieved performance data in 22nm technology node.



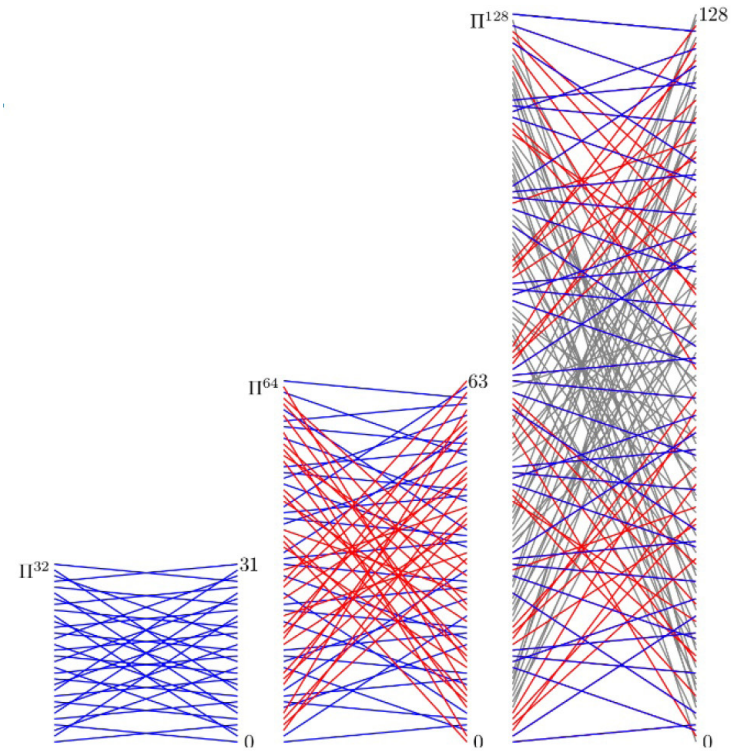
Layout SC-LDPC decoder

| Parameter | Value |
|---|---|
| Window Size [bit] | 5x1280 |
| Iterations | 5 |
| Frequency [MHz] | 400 |
| Latency [ns] | 30.0 |
| Coded Throughput [Gb/s] | 512 |
| Core Area [mm²] | 3.94 |
| Power [W] | 3.13 |
| Energy Eff. [pJ/bit] | 6.11 |
| Area Eff. [Gb/s/mm²] | 130 |

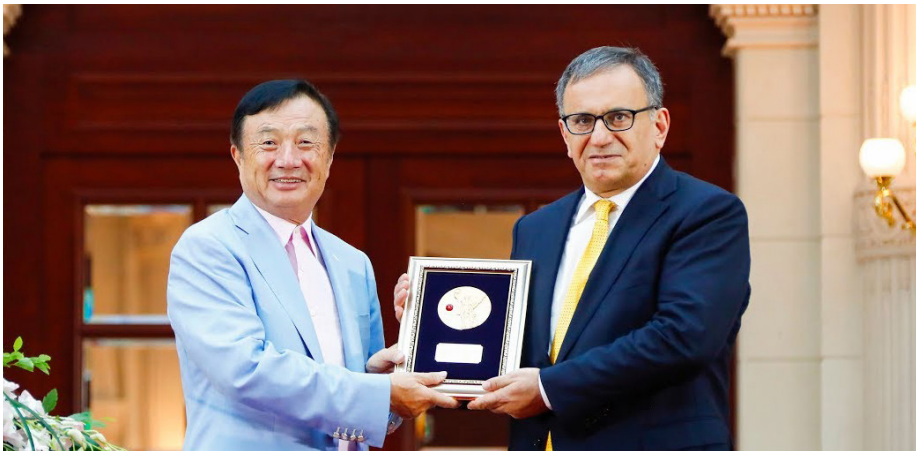
The **Polar codes** are a new era in forward-error-correction. It is a capacity-achieving code with a recursive encoder and decoder structure. The Polar codes are used in 3GPP 5G NR standard for protecting control channels and deliver high-throughput at low energy per bit due to low implementation complexity. For Polar codes, RTL implementation of single-core, 4-core and 8-core designs and corresponding synthesis results were reported in FinFET 16nm. All architectures achieve 1 Tbps throughput after synthesis. The synthesis results show that the 8-core implementation has significantly lower power density than single-core and 4-core implementations. It was observed that as the number of decoder cores increases, there is a diminishing return in terms of power dissipation due to increased complexity of I/O interface with multiplexers.

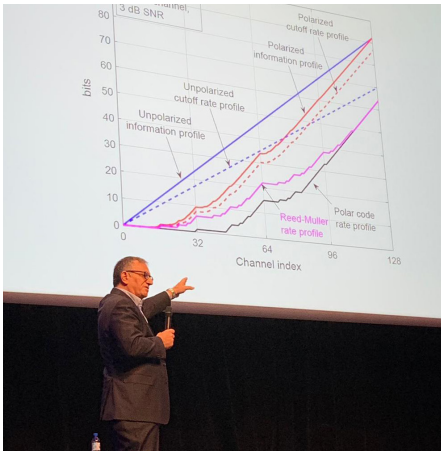


For **Turbo codes**, the architectures are implemented in FD-SOI 28nm. Post place & route results were provided and an improvement of up to 40% in area utilization could be achieved with the new architecture. The investigation of supporting longer code sizes with different X-window sizes reveals the possibility of achieving a throughput of 400 Gbps for code size of 512 in 28nm technology nodes. In addition, the first hardware implementation of non-binary turbo decoder is ready. The architecture exploration phase allowed to propose an original simplification technique in the decoding algorithm leading to significant increase in area efficiency w.r.t. state-of-the-art.



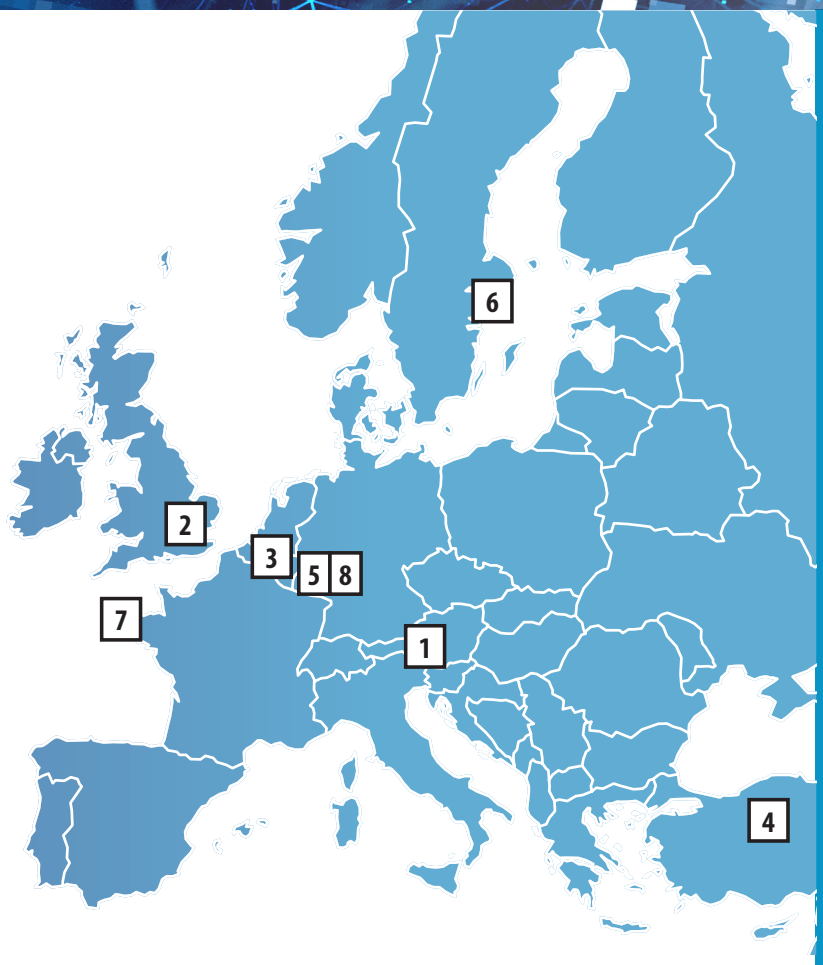

## Dr. Erdal Arikan - honored by Huawei and winner of the Claude E. Shannon Award 2019






Huawei presented a special award to our project partner Dr. Erdal Arikan from Polaran, the inventor of polar codes for 5G, in recognition of his outstanding contribution to the development of communications technology. At the awards ceremony, Huawei founder Mr. Ren Zhengfei presented a medal to Dr. Arikan. The medal, designed and manufactured by the Monnaie de Paris (Paris Mint), features an engraving of the Goddess of Victory with a red Baccarat crystal, symbolizing the importance of new communications technology in leading the world forward.

Further, we are proud to announce that Dr. Arikan won the Claude E. Shannon Award for 2019. The Award of the IEEE Information Theory Society was created to honor consistent and profound contributions to the field of information theory. It is a prestigious prize in information theory, covering technical contributions at the intersection of mathematics, communication engineering and theoretical computer science.




## Project Partners

1 TECHNIKON

2 INTERDIGITAL EUROPE

3 imec

4 POLARAN

5 TECHNISCHE UNIVERSITÄT KAISERSLAUTERN

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7 IMT Atlantique Bretagne-Pays de la Loire École Mines-Télécom

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The EPIC project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 760150.

## Upcoming Events

**3rd Towards Terahertz Communication Workshop**
@ Leuven, Belgium
*The workshop was postponed and the new date will be announced soon.*

**IEEE Wireless Communications and Networking Conference**
@ Seoul, South Korea
*The workshop was postponed and the new date will be announced soon.*

**2nd Workshop on High Throughput Coding**
@ Villejuif Cedex, France
*The workshop was postponed and the new date will be announced soon.*

**International Conference on Acoustics, Speech, and Signal Processing 2020**
**4-8th May 2020**
@ Barcelona/Spain

**IEEE 802 Working Group Meeting**
**10-15th May 2020**
@ Warsaw/Poland

**IEEE International Conference on Communications 2020**
**7-11th June 2020**
@ Dublin/Ireland

**European Conference on Networks and Communications 2020**
**15-18th June 2020**
@ Dubrovnik/Croatia