Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding

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Consortium
8 partners (5 countries)

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www.epic-h2020.eu
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Duration: **36 months**
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EC contribution: **EUR 2,966,268.75**

Message from the Coordinator

This third edition of the EPIC newsletter will focus on dissemination events, that the EPIC consortium attended and what has been displayed at the events.

The EPIC project is on good track – further deliverables have been submitted to the EC on time, risk assessment has been performed and standardization efforts and plans were set out and communicated to the EC.

Further progress has been made during the last technical meeting, which was held in Ankara, Turkey, from the 11th to the 12th of September, 2018, where all consortium members came together to discuss and agree upon the upcoming project plan.

EuMA European Microwave Association

European Microwave Week 2018

CREONIC and IMEC represented the EPIC project at a cluster booth, that was shared between 6 different beyond-5G projects: DREAM, EPIC, TERAPOD, TERRANOVA, ULTRAWAVE, WORTECS. The technical progress of this B5G project cluster has been presented collectively, which presented a valuable collaborative occasion.

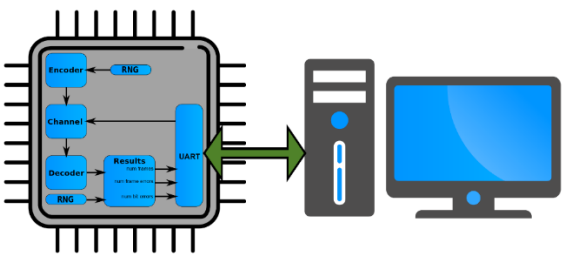
Efficient BER simulation is key for EPIC to assess the performance of the different codes, decoding algorithms etc. Hence, fast simulation is very important.
Creonic presented a FPGA accelerated simulation chain to assess the BER performance of Polar decoding. This simulation chain enables a BER assessment of 10^{-12} in less than 1 minute.

The **EPIC poster** was shown and Creonics presented a demonstrator.
The demonstrator that was shown serves as a proof-of-concept for simulation accelerators, which allows making much faster performance measurements at error rates so low, that would otherwise take much longer times to simulate using only software.

By being able to simulate hundreds of millions of blocks per second, simulation times can be reduced from days to minutes or even seconds, depending on the given settings.

EPIC Project member Jhon Jimenez showing the Demonstrator at the shared booth.

The demonstrator consists of a basic simulation chain implemented onto the FPGA, comprised of an encoder, a noisy channel, a decoder and random data generators.
The endpoint of the chain compares the decoded output against the original data on a frame-by-frame basis and outputs the performance results. These results are fetched from the FPGA and displayed on the computer.
The demonstrator is controlled using a graphical user interface and is set with a non-systematic polar encoder and decoder with a frame size of 128 bits, and rate R = 1/2. The decoder implements Successive-Cancellation-List (SCL) with a list size L = 4 Decoding path. Both the encoder and decoder output one frame per clock cycle.
The chain runs at 300MHz, which translates in a throughput of approximately 19 Gbps, and measurements of error rates as low as 10^{-12} in 1 minute.



Overview of the demonstrator

The performance measurements include

- **Number of frames with errors**
- **Number of bits with errors**
- **Total number of frames**

BER and FER are then calculated using these numbers.

Project Progress

Since the last newsletter, the first EPIC design report has been finalized.
In this confidential report, each task reports on the design space for different code classes, showing the important parameters with regards to communication performance and implementation and identifies the most promising communication and implementation parameters.

It also includes code-specific FEC design framework guidelines. Further, an intermediate standardisation plan has been submitted to the EC, as well as a risk assessment plan, including the critical path of the project.
The consortium is currently working on a Preliminary internal report on link-level simulation performance results, which is due in December 2018.

Project Partners

1 TECHNIKON

2 INTERDIGITAL EUROPE

3 imec

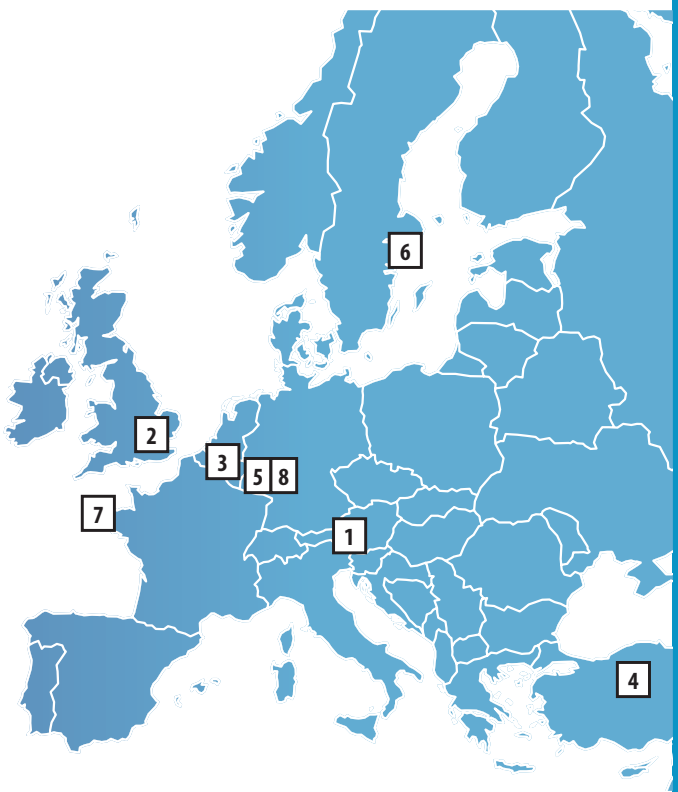
4 POLARAN

5 TECHNISCHE UNIVERSITÄT KAISERSLAUTERN

6 ERICSSON

7 IMT Atlantique Bretagne-Pays de la Loire École Mines-Télécom

8 CREONIC



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The EPIC project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 760150.

Past Events

IEEE 802.15 Plenary Meeting - 8th to 13th July 2018
@ San Diego, USA

IDCC attented the Meeting.

EuCNC - 18th to 21th June 2018
@ Ljubljana, Slovenia

TUKL and IDCC presented the EPIC project in a special session called "SP3: Terabit Wireless Transport for Networks Beyond 5G." A scientific paper was accepted in the conference proceedings.

Upcoming Events

IEEE WLAN Pleanary Session 172 - 11th to 16th November 2018
@ Bangkok, Thailand

IDCC will attend the Meeting

Information Theory Workshop - 25th November 2018
@ Guangzhou, China

Prof. Erdal Arikan from Polaran will give an invited talk on polar coding

IEEE Globecom 2018 - 9th to 13th December 2018
@ Abu Dhabi, UAE

Partner TB will give a presentation: „Design of Low-Complexity Convolutional Codes over GF(q)"

ISTC 2018 - 3rd to 7th December 2018
@ Hong Kong, China

Partners will participate in special sessions. Prof. Norbert Wehn and Prof. Erdal Arikan will also give invited talks at the conference.