Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding

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Consortium
8 partners (5 countries)

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Message from the Coordinator

In this second edition of the EPIC newsletter, we would like to focus on standardisation efforts and contributions to standards, within the EPIC project.

The EPIC project is off to a good start – several deliverables have been submitted to the EC and the basis for progress has been set during the previous technical meeting, which was held in Berlin, Germany from the 7th to the 8th of March.

Further, B5G wireless TB/s use-cases and FEC KPI parameters have been set and finalized and SoA FEC gap analysis was succefully carried out within the project.

EPIC Contributions to THz Standards

The technological progress on various fronts of THz and ultra-high throughput systems has placed the standardization efforts on the topic into the spotlight recently. The significance of such efforts, whether under existing standardization bodies or to-be-established groups, is deemed to only increase in the near future.

In the light of an exciting era in the standardization that is about to kick off soon, the EPIC project, with its main objectives, is positioned to be part of these developments with its active contributions.

It is well-known that the ultra-high throughput wireless systems (e.g. above 100Gb/s) as well as THz operations are open to significant technical challenges that need to be overcome.

The baseband design and development stands as a major challenge among others, where a practical Forward-Error-Correction (FEC) element is the vital component of the base-band sub-system.

Due to the obvious potential of THz systems, thanks to abundant available bandwidths in those frequencies, the first official interest group on this technology in fact dates back to almost a decade now.

We see the initial coordinated actions of roadmap studies and contributions under **IEEE 802.15 THz Interest Group** around the year 2008.

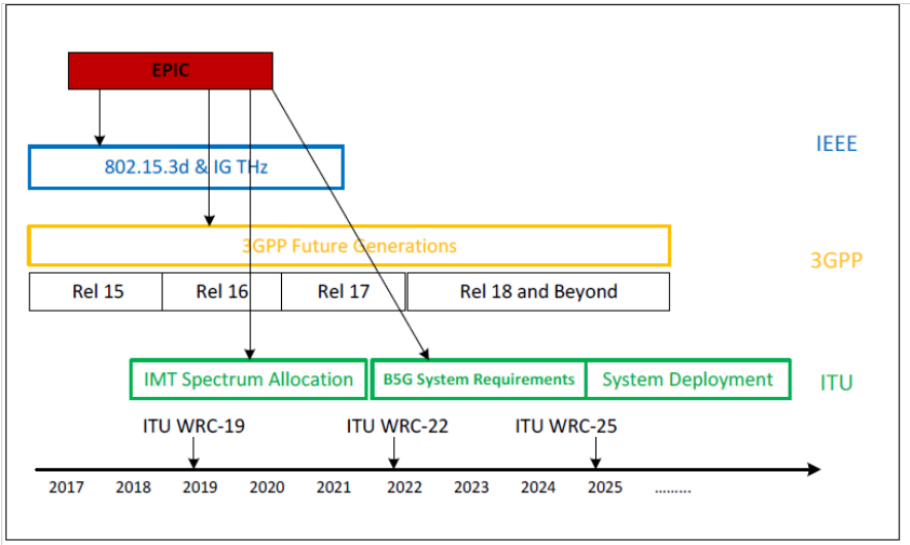
Over the last decade, with the surge of enabling technical components, e.g. device-level, algorithmic, as well as spectrum allocation developments, this collaborative effort has resulted in an officially approved specification named IEEE Std 802.15.3d-2017, which is an amendment to the High Rate Wireless Personal Area Network (WPAN) Task Group (TG), also called as **IEEE 802.15.3 standard**. More specifically, IEEE Std 802.15.3d-2017 aims at an alternative physical layer (PHY) at the lower THz frequency range between 252 GHz and 325 GHz for switched point-to-point links. The specification defines two PHY modes that enable data rates of up to 100 Gb/s using eight different bandwidths between 2.16 GHz and 69.12 GHz.

In the future releases of a THz based standardization, throughputs well approaching Tb/s data-rates are considered as highly possible which is depicted by several recent contributions on the topic.

On **the cellular standardization front**, 3GPP 5G progress has focused on high-throughput use-cases under the umbrella case denoted as eMBB, as well as ultra-reliable low-latency communications (URLLC), and massive machine type communications (mMTC). In terms of high throughput technology, the eMBB aims at peak throughputs around 20Gbps for 5G standards.

However, in the future releases of 3GPP, e.g. Release 17 and beyond, a throughput scaling of 10x is deemed a reasonable target as it is manifested in several release cycles.

Therefore, ultra-high throughput systems and their enabling technologies, potentially under THz or millimetre waves (mmW) with advanced massive MIMO and bandwidth ag-



EPIC Project and the anticipated wireless B5G standardization timeline

gregation techniques, can be expected to be a key topic in the leading cellular standardization body, 3GPP.

The EPIC project, which is still yet to complete its first year in September 2018, has **already started active participation with contributions to the relevant standard groups.**
In this regard, the EPIC project, represented by IDCC and IMEC, has attended the IEEE 802.15 THz IG Meeting, from the 7th to 8th of May, 2018 in Warsaw, Poland. The attendance has been complimented with two contributions that were presented in the THz IG meeting and the contribution slides are published and now included in the IEEE standardization repository.
The first contribution details the project content and objectives, with the ultimate target of **design and implementation of practical ultra-high speed FEC technology for B5G systems**. It further provided a detailed design framework of leading codes, Turbo Codes, LDPC, and Polar Codes along with various parameters (aka the design space exploration (DSE)) based on the inherent trade-offs between the coding theory and efficient FEC architecture design.
In the second contribution, an overview of the state-of-the-art (SoA) high throughput FEC implementation results of these codes in the current 28nm technology is presented.
Furthermore, the contribution summarizes a detailed study in EPIC project which demonstrates the anticipated performance gaps between potential requirements of practical wireless Tbps use-cases and the 7nm performance extrapolation of SoA high throughput FEC.
This study demonstrates the order of performance gaps between today's most advanced codes and the partical requirements of ultra-high throughput systems. The observed performance gaps clearly shows the necessity to design and develop new codes for ultra-high speed beyond-5G technologies.
In the upcoming periods, the participation and contributions of the EPIC project is due to continue at an increased pace.
As the initial technical motivations to design and develop novel B5G FEC technologies are laid out, the EPIC project aims at providing technology solutions towards this challenging target.
These solutions are already in the making by the EPIC consortium as a whole as well as by individual partner contributions to the standards.

Past Events

IEEE 802.15 THz Working Group Meeting - 7th to 10th May 2018
@ Warsaw, Poland

Wireless Communications and Networking Conference - 15th April 2018
@ Barcelona, Spain

Thz Workshop IMEC - 7th March 2018
@ Brussels, Belgium

IEEE International Workshop on Signal Processing Systems (SiPS) - 3rd to 5th October 2017
@ Lorient, France

Upcoming Events

ISTC International Symposiom on Turbo Codes & Iterative Information Processing - 3rd to 7th December 2018
@ Hong Kong, China

EuCNC - 18th to 21th June 2018
@ Ljubljana, Slovenia

Next-Generation Channel Coding Towards Terabit/s Wireless Communications

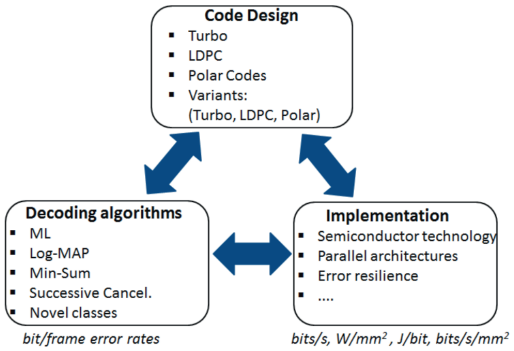
The continuous demands on increased spectral efficiency, higher throughput, lower latency and lower energy in communication systems impose large challenges on the baseband processing in wireless communication.
This applies in particular to channel coding (Forward Error Correction), a core technology component in any digital baseband. Future Beyond- 5G use cases are expected to require wireless data rates in the Terabit/s range in a power envelope in the order of 1-10 Watts. Microelectronic improvement can no longer keep pace with the increased requirements from communication systems.
Advanced technology nodes imply new challenges such as reliability, power density, cost etc. Thus, channel coding for Beyond-5G systems requires a real cross layer approach. The EPIC project aims to develop new Forward Error Correction (FEC) schemes for future Beyond-5G use cases targeting a throughput in the Tb/s range. **Focus will be on the most advanced FEC schemes: Turbo codes**, Low Density Parity Check **(LDPC)** codes and **Polar codes.**

In the foreseeable future, progress in microelectronics will yield some improvements in the three important metrics, i.e.area, energy, and frequency. Power density will be one of the largest challenges and is already a big issue in today's technologies, which is known as "dark silicon phenomenon" for beyond-5G FEC.
Improvement from new silicon technology has to be complemented with improvements on the code level, the decoding algorithms and the architectural level.

Implementation Challenges

To bridge the gap between information theory and efficient implementation EPIC pursues a holistic approach in which information theory, code design, algorithms/architecture co-design, front-end and back-end implementation optimization are considered together.

Verification and Ranking of FEC Algorithms is EPIC's core step in which the aforementioned holistic approach is pursued for the three different advanced coding schemes: **Turbo codes, LDPC codes and Polar codes.**
The investigation starts with the definition of use cases and corresponding Key Performance Indicators (KPIs). EPIC identified a set of Beyond-5G use cases by analyzing state-of-the art literature and current standardization efforts. In total eight Beyond-5G use cases were identified. We considered only use cases that are particularly interesting and challenging in the context of advanced FEC technologies. The selected use cases are data kiosk, virtual reality, intra-device communication, wireless front-haul/backhaul, data center, hybrid fiber-wireless networks, high throughput satellites. For all use cases key performance indicators were determined.



EPIC FEC design framework

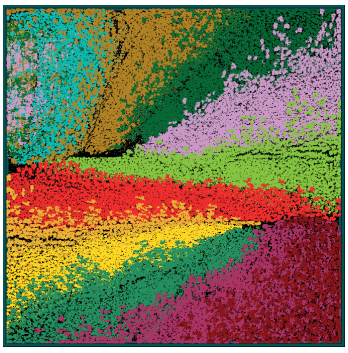
These KPIs are divided into two sets: communication/ system performance and Implementation. Corresponding implementations KPIs were calculated for two technology nodes: 28nm that is state-of-the-art technology for many published FEC IPs and for a projected advanced 7nm technology node.
KPIs were analysed for the 7 EPIC use-cases and the **following targets were fixed for the EPIC project**: meet the communication performance requirements for Beyond-5G use cases and at the same time, an area efficiency of 100 Gbit/s/mm^2, an energy efficiency of about 1pJ/bit and a power density in the order of 0,1W/mm^2 for a 7nm technology node.

High-Throughput Decoders

The challenges for high-throughput decoder implementations are fundamentally different between Turbo codes, LDPC codes and Polar codes resulting in a large difference in the achievable throughput and energy efficiency of today's state-of-the-art decoders.

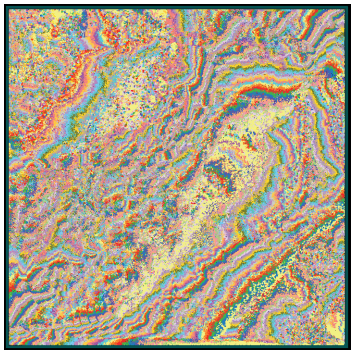
The two most prominent techniques to achieve high- throughput on architectural level are **spatial parallelism and functional parallelism (pipelining).** Pipelining has some efficiency advantages, i.e. large locality, compared to spatial parallelism, but is limited in its applicability if control-flow, e.g. iteration control, plays a major role.

In addition, in pipelined architectures throughput is increased at the cost of additional storage since several blocks have to be kept simultaneously in the pipeline stages. Thus deeply pipelined architectures can suffer from large storage requirements that are a major source of power consumption. **Channel decoding algorithms are mainly data-flow dominated.** To achieve throughput far beyond 100 Gbit/s, dataflow and tree structures must be flattened, or "unrolled", and pipelined respectively. Here we present two high-throughput decoders that are based on this principle.



Layout LDPC code decoder in 28nm. Area is 2.8 mm². The different colors represent the different decoding iteration (in total 9 iterations)

The first decoder is an LDPC decoder supporting the 802.11ad standard. The decoder was synthesized on a 28nm Fully DepletedSilicon on Insulator (FD-SOI) technology under worst case Process, Voltage and Temperature (PVT) assumption. The decoder was characterized for different voltages. Extrapolating outcomes at these different voltages to 7nm gives a throughout of 480 Gbit/s and 1.5 pJ/bit.



Layout Polar decoder. Area is 4.3 mm². Code block 1024, Rate=0.5. Each color represents a stage in the factor tree traversal (in total 385 stages).

The second decoder is a Polar code decoder advising a throughout of 620 Gbit/s. Decoding is performed with the successive cancellation algorithm. This decoder was synthesized on the same technology and under the same conditions as the LDPC decoder. Extrapolating achieved numbers to the 7nm with a maximum frequency of 1Ghz results in an energy efficiency of less than 2 pJ/bit.

The presented decoder architectures demonstrate that unrolled **dataflow architectures allow very high throughput approaching the 1Tb/s wall in 7nm technology.** However, there are trade-offs between communication performance and high throughput that depend on the particular use case.

High communication performance typically requires complex decoding algorithms to achieve near maximum-likelihood performance and large block lengths to approach the Shannon bound. But unrolling under 1GHz frequency and area constraints is only feasible for smaller block lengths and limits the complexity of the decoding algorithms.

Furthermore, unrolled architectures suffer on flexibility. Therefore **the biggest implementation challenge is achieving the requirements on energy efficiency and power density while maintaining communication performance and the necessary flexibility required by the use cases.**

The **EPIC project** is dedicated to tackle these challenges by utilizing its holistic implementation-aware channel code design framework and to **develop one of the first Beyond-5G FEC technology solutions.**

Project Progress

A report on B5G Wireless Tb/s FEC KPI Requirements and Technology Gap Analysis was finalized. It determines the FEC performance requirement set for the EPIC projects and wireless Tb/s use-cases in general.
This report sets the performance targets for the FEC development work in the rest of the project. **(Link: https://epic-h2020.eu/downloads/EPIC-D1.2-B5G-Wireless-Tbs-FEC-KPI-Requirement-and-Technology-Gap-Analysis-PU-M07.pdf)**

Further, a report on link level simulation methodology for the evaluation and comparison of the FEC codes was successfully completed: It reports on link-level simulation methodology for the evaluation and comparison of the FEC codes. It describes the common link-level simulation template and the common calibration plan as well as the simulation plan.
Moreover, a First Design Report has been finalized: Each task reports on the design space for the different code classes showing the important parameters with regards to communication performance and implementation, and identifying the most promising communication and implementation parameters. Code-specific FEC design framework guidelines are also included here.

Submitted public deliverables

D1.2 B5G Wireless Tb/s FEC KPI Requirments and Technology Gap Analysis

Scientific Publications

Protograph-Based Interleavers for Punctured Turbo Codes (December, 2017)

Ronald Garzón Bohórquez, Charbel Abdel Nour, Catherine Douillard

Advanced Wireless Digital Baseband Signal Processing Beyond 100 Gbit/s (October, 2017)

Stefan Weithoffer, Matthias Herrmann, Claus Kestel, Norbert Wehn

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